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Variability Analysis and Modeling of The Crosstalk Effects on The Low-Swing Signaling Scheme using DOE Approach

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Abstract—Through aggressive technology scaling, the continuous demands of devices with interconnect functionality/unit area have been satisfied but with adversely negative impact on the interconnect delay. This trend also has made reliability a huge challenge for the designers. This reliability comes in the form of process variation which can have significant impact on the interconnect delay, specifically the crosstalk delay. A statistical analysis using a Design-of-Experiment method was carried out to create models which can represent the effect of process variation on the crosstalk delay as well as crosstalk noise on low-swing signaling scheme; highlighting on the most significant parameter variations, which are Vdd and wire parameters and methods to reduce the crosstalk effects.

Keywords: low-swing, design-of-experiment, variability, crosstalk effects, crosstalk capacitance.

1. INTRODUCTION

Technology scaling has always been an important issue for microprocessor especially in deep submicron regime. Besides from the aggravating effect of the market demands for increased functionality per unit area on the interconnect delay, there are two other significant performance impacts resulting from this, i.e. the variability and the crosstalk effect. The variations in process and design parameters have significantly increased due to the rapid scaling of *CMOS* technology which leads to severe variability in circuit performance and functionality in the nano-metre regime [1]. As device sizes continue to scale down into the deep submicron regime, manufacturing tools are less reliable in their control of design parameters. Process variation usually arises from limitations imposed by the layers of physics, imperfect tools and properties of materials that are not fully understood [2].

Subsequently, as the feature sizes have been shrinking with process technology scaling, the spacing between adjacent interconnect lines keeps decreasing in every process node. While the lateral width of interconnect wires has been scaled down significantly, their vertical height has not been scaled in proportion, which leads to a very rapid increase in the amount of coupling capacitance between the wires. More aggressive technology scaling will lead to an increase in the overall contribution of the coupling capacitances to the total interconnects capacitance. Subsequently, as technology advances, there will be an increase in chip frequency and decreases in voltage margin, which will exacerbate the impact of crosstalk noise on interconnect delay. All the above trends consolidate the needs to include crosstalk effect in the reliability analysis of *VLSI* circuits.

This paper will discuss on the impact of parameter variations on the crosstalk delay and noise using Design-of-Experiment (DoE) approach where relationships between the parameter variations as well as to the crosstalk effects will be identified. The interconnect scheme to be analysed is the mLVSD scheme where the preliminary analysis in [3,4] indicated that this scheme has the best attributes among the low-swing signalling schemes.

Section II begins with introduction of the diode-connected driver scheme, i.e. the mLVSD driver. This is followed by the method flow for variability analysis using the DoE method. This method flow can also be implemented on other low-swing signalling scheme. This is followed by the analysis and modelling of crosstalk effects on the mLVSD scheme where the most significant parameters will be identified.

2. THE DIODE-CONNECTED DRIVER SCHEME

The concept of a low-swing driver, realised in the mLVSD driver is adapted from an up-down low-swing voltage driver (UDLD) shown in Figure 1[5], where the output voltage swing of these drivers is based on the value of the threshold voltage. This is simply categorised as diode-connected configuration. In the diode-connected configuration the drain terminal of a device is shorted to the gate terminal, subsequently the drain saturation current, I_{dsat}, which flows through the *MOSFET* device increases exponentially with the increase in the output voltage. The I-V characteristics for this configuration are qualitatively similar to a p-n junction diode or *MOS* diode, which is mostly used as a component in a current mirror or a means of creating a voltage drop in level translation circuit. The nature of this configuration is that it is able to control the output to a certain voltage level and not allow that voltage to increase beyond a given limit. Basically it compresses the input voltage into a smaller output voltage; hence a low swing signal is produced. At low voltage levels, I_{dsat} can be reduced significantly to freely change the value of the output voltage with little or no impedance loading [5]. For deep submicron processes, the resistivity of the interconnect is significant and over-driving the interconnect by actively driving the interconnect beyond the low swing limits will help in decreasing the propagation delay. The amount of over-drive is determined by proper transistor sizing.

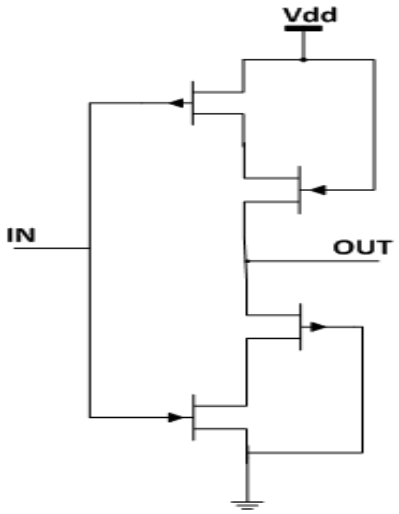


Figure 1: Circuit diagram of the UDLD driver

The diode-connected driver has been qualitatively compared with other low-swing signalling schemes such as the differential current mode technique [6] or driver pre-emphasis driver [7] and

tabulated in [3] where the result indicates that the diode-connected driver, has the best attributes compared to the other signalling schemes. This is because the scheme provides low power and high speed signalling without the use of extra circuitry such as extra V_{dd} and reference voltages. There are three types of low-swing driver that incorporate diode-connected configuration in their circuits, i.e. the MJ [8], nLVSD [3] and mLVSD drivers.

Further comparison in [3] indicates that the circuit structure in the MJ driver, which employs multipath feedback technique, is considered to be redundant in terms of area and time as only half of the circuit is needed to be operational during each rising and falling transition. Thus in [9] a new low-swing signalling scheme with a diode-connected configuration, known as the nLVSD driver was proposed to eliminate these disadvantages as well as improve its power consumption and delay of the circuit. This driver has shown a significant improvement with 34% in power consumption and 28% in delay over the MJ driver. However due to its low voltage swing, the noise immunity of the nLVSD driver is considered to be poor, thus mLVSD is proposed which incorporates all of the essential components of diode-connected driver as in the nLVSD circuit with similar structure as shown in Figure 2(a). The mLVSD driver is less affected by the noise due to its voltage swing, which is higher than the nLVSD but smaller than the MJ driver, thus maintaining the low power consumption whilst improving the robustness against noise.

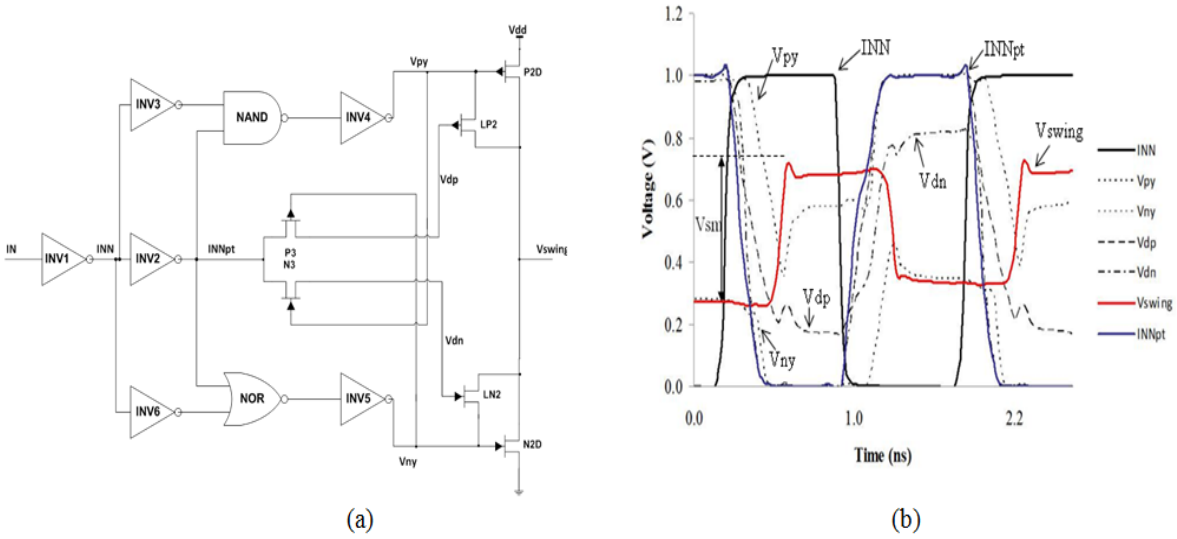


Figure 2: (a) Circuit diagram and (b) signal waveforms of the mLVSD driver

Similar to the nLVSD driver, the mLVSD employs a diode-connected transistor pairs at the output. However the difference between the two drivers is the output voltage swing of the mLVSD driver is not dependent on a set of drivers; INV4 and INV5, up-sized and down-sized drivers, but instead follows the changes in the input to the pass transistor pairs (N3,P3). Figure 2(b) indicates the voltage swing of the mLVSD is higher compared to the nLVSD ($V_{sm} > V_{sn}$) since the output voltage swing is no longer dependent on INV4 and INV5, or limited by the value of V_{py} and V_{ny}. Thus the output swing is no longer range from $V_{py} - V_{th}$ and $V_{th} - V_{ny}$ like the nLVSD driver, but encapsulates the same voltage swing range as the typical diode-connected driver, e.g. UDLD circuit, which is from V_{thn} to $V_{dd} - |V_{thp}|$. The mLVSD driver is known to be more stable than the nLVSD driver as the output voltage swing will never reached below the threshold voltage, thus improving the noise immunity as well as providing low power and high speed signalling.

3. WORK FLOW FOR VARIABILITY ANALYSIS IMPLEMENTING DOE METHOD

The work flow for the variability analysis used in this paper is summarised below:

3.1. Modelling the parasitic elements of the circuit

The interconnection between driver and receiver in the signalling scheme is implemented using top layer metal to be realised using *UMC* 90 nm technology. A three-wire signalling arrangement with crosstalk effects is set up for the experiment as shown in Figure 3. The parallel line structures are placed between two grounded shields. The resistive and capacitive parasitic elements of the interconnect are calculated using the following equations.

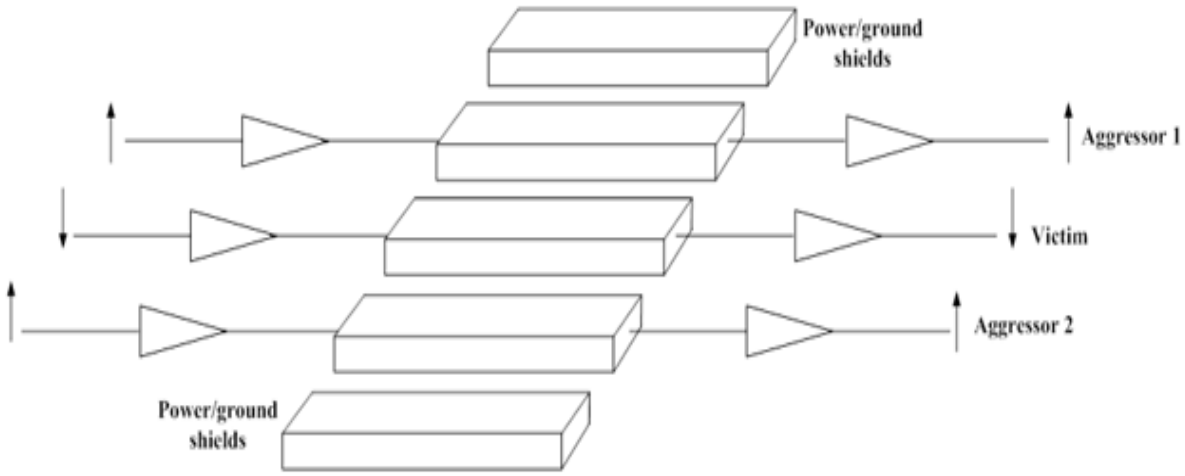


Figure 3: Circuit structure for variability analysis on crosstalk effects

C_{wire} is the parasitic capacitance, which is a very strong function of the geometry. For the configuration of a conductor surrounded by two adjacent wires as shown in Figure 4, Sakurai in [10] defines a coupling capacitance as follows:

$$C_g = \varepsilon_k \left[1.15 \left(\frac{w}{h} \right) + 2.4 \left(\frac{t}{h} \right)^{0.222} \right] l_e \tag{1}$$

$$C_c = \varepsilon_k \left[\begin{array}{c} 0.003 \left(\frac{w}{h} \right) + 0.83 \left(\frac{t}{h} \right) \\ -0.07 \left(\frac{t}{h} \right)^{0.222} \end{array} \right] \left(\frac{h}{s} \right)^{1.34} l_e \tag{2}$$

$$C_{wire} = C_g + 2C_c \tag{3}$$

where ε_k is dielectric permittivity, h is dielectric height and s is separation between two wires. C_{wire} defines a total capacitance for the middle conductor as the sum of C_g and $2C_c$ assuming that there is no signal transition on the two adjacent wires. The resistance can be obtained through [11],

$$R_w = \frac{pl_g}{wt} \tag{4}$$

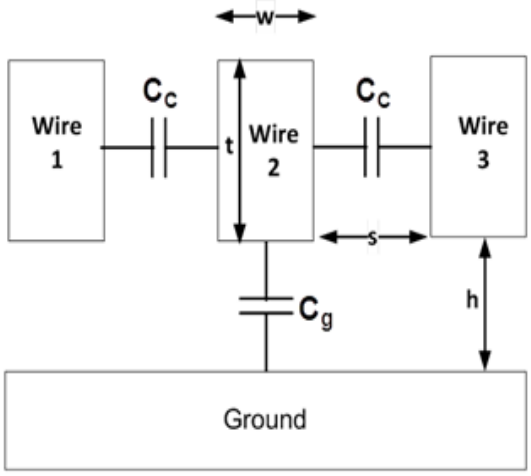


Figure 4: Cross-section of wire capacitance [11]

where ρ is the metal resistivity, l_e is the interconnect length, while w and t, are the interconnect width and thickness respectively. The interconnect model for this work is calculated to comprise a 567.9 Ω resistor and a 2.2356 pF capacitor to represent an interconnect length of 10 mm using nominal values of interconnect parameters recorded in Table 1 at 90 nm technology. The wire capacitance is calculated using the equations given with $C_g = 0.307$ pF and $C_c = 0.964$ pF. An extra load capacitance, C_l of 0.25 pF per mm length of interconnect is also distributed along the wire to represent the fan-out.

Table 1: Nominal values of interconnect parameters

Parameters	Nominal values
Interconnect width, w	0.56 µm
Interconnect thickness, t	0.81 µm
Interlayer dielectric height, h	0.94 µm
Metal resistivity, ρ	21.8 nΩ.m
Dielectric permittivity, k	3.25

3.2. Identify sources of variation

In this work, Plackett-Burman design was carried out on 31 devices and interconnect parameters associated with the low-swing driver schemes. Through Plackett-Burman screening the main effects or factors has been reduced to 12 as listed in Table 2 with their 3σ variations, these values are in

agreement with those used previously [11].

The device parameters include the threshold voltage, *Vtho*, gate-oxide thickness, *tox* and other parameters such as carrier mobility, μo and effective gate length, *Leff*, whilst the interconnect parameters are as mentioned previously. Environmental factors such as *Vdd* and temperature are also included in the variability analysis.

Table 2: Parameter values and 3σ variations

Technology		**90 nm**	
Device parameters	±3σ	Interconnect parameters	±3σ
Vth	30%	ε_k	3%
tox	10%	ρ	30%
Leff	16.7%	*s*	20%
μo	10%	*w*	20%
Vdd	10%	*t*	10%
Temp	(12-70)°C	*h*	10%

3.3. Design of the statistical experiment

DoE techniques are employed in the variability analysis of the mLVSD driver scheme in order to build a first order polynomial approximation for the first set of experiment and a second order polynomial approximation for the design metric of interest which is the crosstalk delay. For the 12 input parameters used for this analysis, DoE technique used here requires 154 experiments.

3.4. Record circuit response at each design point

In order to obtain the circuit response for each design point, simulations are carried out using the circuit analyzer (SPECTRE) in Cadence Virtuoso Analog Design Environment. The crosstalk effects were measured and calculated in each experiment.

3.5. Generate polynomial approximations for the circuit output

The polynomial approximations are obtained through statistical software called *Minitab*. The coded polynomial approximation is used. The input factors in the coded approximation have normalized values of (-1, 0, +1) which represent $(\mu - 3\sigma,\ 0,\ \mu + 3\sigma)$, where μ and σ are mean and standard deviations of the input parameters to be tested.

The following sections outline the results obtained from the methodologies used, to analyse the impact of variability on the crosstalk delay and noise of the mLVSD driver. Design models for the driver scheme are also discussed for each set of experiments.

4. ANALYSIS AND MODELLING OF CROSSTALK DELAY AND NOISE ON THE MLVSD DRIVER SCHEME

For simplicity, in the following analysis, 8 sources of variations were considered, namely, *Vdd*, temperature, *Vth*, *Leff*, ρ and wire (w, t, h). The wire width and spacing are assumed to be negatively correlated, letting w be the independent variable. The same goes for *Vth* as it is used instead to represent both *Vtho* and *tox*. The variables were listed previously in Table 2 with their 3σ variations. The wire width used in this analysis is the minimum wire width in 90 nm technology. The variability analysis was carried out for both, the crosstalk delay and noise, which will be further discussed separately.

4.1. Impact of variability on crosstalk delay

Figure 3 shows the interconnect structure used in the analysis of the impact of process variation on crosstalk effects. The DoE method outlined previously is used in this analysis to build a linear model based on the model in [12]. In this instance the linear model of the delay of the middle (*victim*) line in Figure 3 is given by

$$D = \beta_0 + \beta_1 x_1 + \beta_2 x_2 + \cdots + \beta_i x_i \tag{5}$$

where x is a variation parameter, which in this case are *Vdd*, *Temp*, *Leff*, *Vth*, ρ, w, t and h, and β is a regression coefficient.

There is several design methods that can be implemented in mitigating the problems associated with crosstalk delay. The same methods are also considered in the variability analysis of crosstalk delay, namely, buffer insertion and increased wire spacing. Subsequently, general models for a 10mm interconnect were generated for the following cases: minimally spaced wire ($s = wmin$) with no buffers, minimally spaced wire with 3 buffers and 3 times minimally spaced wires ($s = 3wmin$) with no buffers. The accuracy of these models was validated using R^2 fits analysis, which was found to be above 99% for all considered cases. R-squared (R^2) is percentage of response variable variation, which is always between 0% and 100%. In general, the higher the R^2, the better the model fits the data. Similar models are also generated for each crosstalk cases as shown in Table 3 indicating effective crosstalk capacitances for different crosstalk cases [13]. Notes that ↑, ↓ and - imply 0-to-1, 1-to-0 and no transitions respectively.

As expected, delay sensitivity to variation parameters increases from Crosstalk Case 2 to 5 due to the increase in effective crosstalk capacitance. In Figure 5 represents delay sensitivity over the variation parameters, where the results were obtained through Minitab. From Figure 5(a), the results indicate that both *Vdd* and ρ have the highest impact on crosstalk delay variations as both of these parameters have the most significant association with delay. Delay is linearly dependent on the wire resistance as well as being negatively correlated to *Vdd*. Subsequently this result also shows that delay sensitivity to wire parameter variations has a very high data dependency due to the changes in the effective crosstalk capacitance for each different case. This dependency can be reduced by incorporating 3 buffers on the interconnects, by the significant decrease in delay sensitivity to wire parameter variations. By increasing the wire spacing, the dependency of delay sensitivity on wire parameters can also be reduced but not as much as using the buffer insertion method as shown in Figure 5(c); however, this method can be used to reduce the delay sensitivity to device parameters. This is because by increasing the wire spacing, contributing to the decrease in delay by reducing the wire capacitance without affecting its resistance, which causes the contribution of the driver circuitry to the overall delay to be reduced.

In addition to the first order model generated, a second order model of the crosstalk delay can also be generated. This model comprises interaction and quadratic effects between parametric variations, where its polynomial approximation is based on

$$D = \beta_0 + \beta_1 x_1 + \beta_2 x_2 + \beta_{11} x_1^2 + \beta_{22} x_2^2 + \beta_{12} x_1 x_2 \tag{6}$$

Table 3: Effective crosstalk capacitance for different crosstalk cases

Crosstalk case	Transitions	Effective Coupling Capacitance
1	↑↑↑, ↓↓↓	0
2	↑↑–, –↑↑ ↓↓–, –↓↓	1
3	–↑–, –↓– ↓↑↑, ↑↓↓ ↑↑↓, ↓↓↑	2
4	↓↑–, –↓↑ –↑↓, ↑↓–	3
5	↓↑↓, ↑↓↑	4

where x is a variation parameter, which in this case are *Vdd*, *Temp*, *Leff*, *Vth*, ρ, w, t and h, and β is a regression coefficient, whilst the three added terms, namely $\beta_{11}x_1^2, \beta_{22}x_2^2$ and $\beta_{12}x_1x_2$. The results obtained though Minitab for the non-linear model are presented in Figure 4 where $\beta_{11}x_1^2$ and $\beta_{22}x_2^2$ represent the quadratic effect of the parameter whilst $\beta_{12}x_1x_2$ represents interaction effect.

A comparison between second order and linear coefficients from Figure 5 indicates that the linear coefficients are more significant. Subsequently most of the non-linear effects can be ignored as they have very little impact on the model accuracy. However, as can be seen in Figure 6(a) the quadratic effect of *Vth* is relatively large representing the only significant parameter from the device parameter variations while from the interconnect parameters, the quadratic effects of wire width and dielectric thickness are found to be significantly large. This is because of the dependency of voltage swing on *Vth*, which can affect the delay significantly, and the quadratic effects of w and h contribute to the changes in effective crosstalk capacitance, hence deviations in crosstalk delay. Additionally, the interaction between *Vdd* and ρ also contribute to the large coefficients for delay sensitivity. From Figure 5(a), both *Vdd* and ρ are the most significant parameters to affect delay sensitivity, thus their interaction will have large impact on the delay sensitivity.

4.2. Impact of variability on crosstalk noise

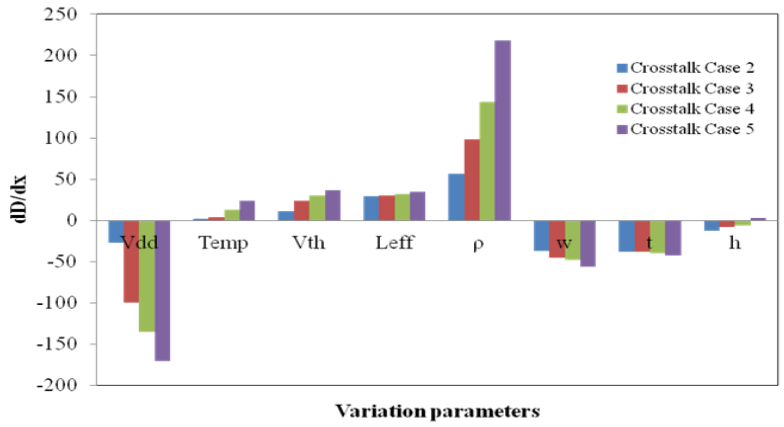
The DoE (CCD) technique was employed in this analysis to build a polynomial approximation of the crosstalk glitch induced on the middle line in Figure 3. There are three types of crosstalk glitches resulting from:

Case 1: the switching of two aggressor wires in different directions

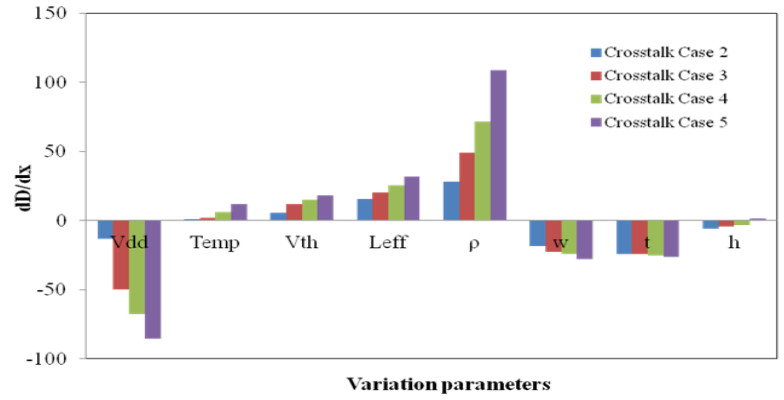
Case 2: the switching of one aggressor wire

Case 3: the switching of two aggressor wires in the same direction

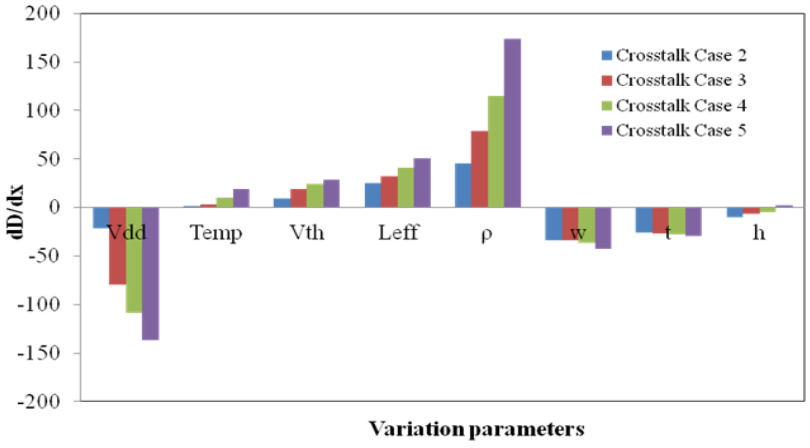
However, the crosstalk glitch resulting from the switching of two aggressor wires in different directions is ignored as its impact is considered insignificant, thus only cases 2 and 3 are considered in this analysis. In order to investigate the sensitivity of the glitch to parametric variations, linear models of crosstalk glitch in each case are generated for minimally spaced wire with no repeaters.



(a)

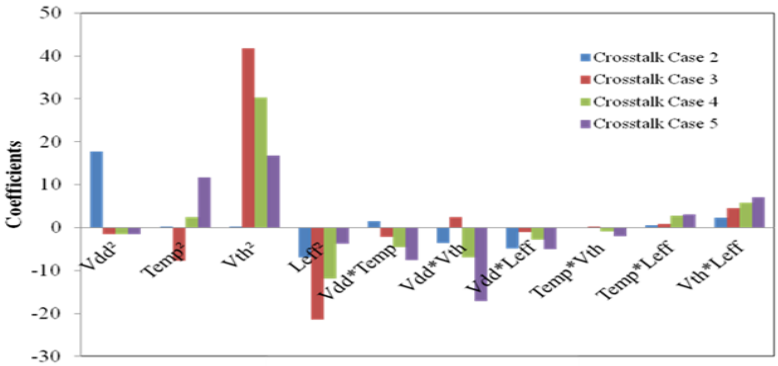


(b)



(c)

Figure 5: Delay sensitivity to variability of (a) a minimally spaced wire with no buffer, (b) a minimally spaced wire with 3 buffers and (c) a 3 times minimally spaced wire with no buffer



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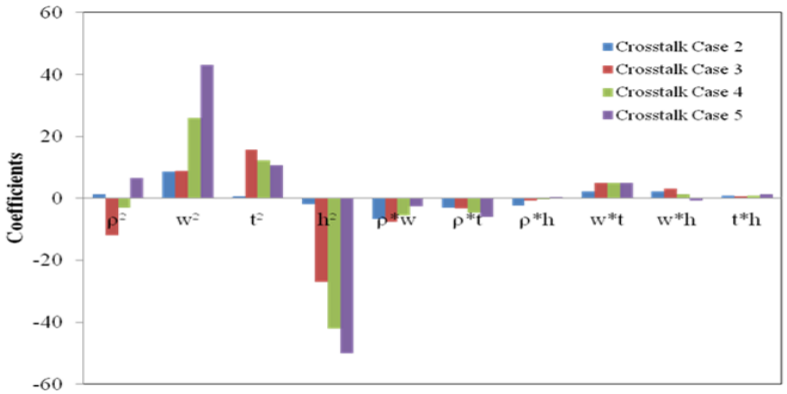

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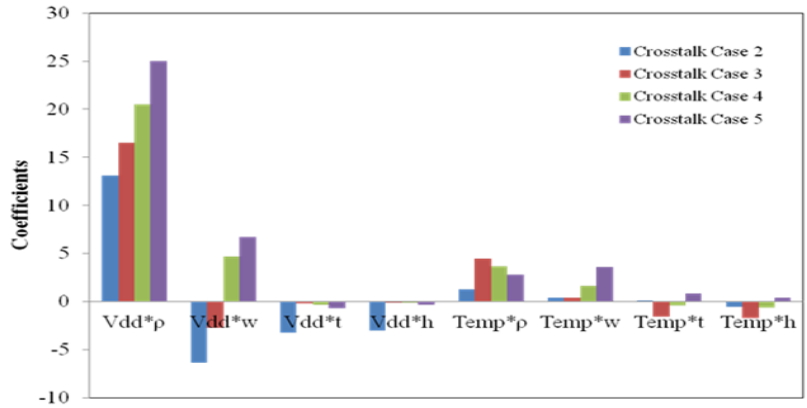

(c)

Figure 6: The results show the interaction and quadratic coefficients of (a) device and environmental parameter variations and (b) wire parameter variations; and interaction coefficients of (c) wire and environmental parameter variations

The polynomial approximation of the linear model used to represent the crosstalk glitch is given by Eq. (7).

$$G = \beta_0 + \beta_1 x_1 + \beta_2 x_2 + \cdots + \beta_i x_i \tag{7}$$

where G represents the crosstalk glitch, x_i represents variation parameter which in this case are *Vdd*, *Temp*, *Leff*, *Vth*, ρ, w, t and h, and β_i is regression coefficient for each variation parameter respectively. R^2 was found to be around 99% for all cases.

From Figure 7, the results indicate sharp increases in crosstalk glitch sensitivity to all variation parameters in Cases 2 and 3. Figure 7 and 8 represent glitch sensitivity over the variation parameters, where the results were obtained through Minitab. Crosstalk glitch sensitivity to wire parameter variations has a very high data dependency especially w, which is one of the main contributors to effective crosstalk capacitance. However, changes in *Vdd* have also a sizeable contribution to the overall variations. These results are supported by their linear relations to the crosstalk glitch, as shown below [14]:

$$G = V_{peak} = V_{dd} \times \frac{c_c}{t_{aggressor}} \times R_{victim} \tag{8}$$

where C_C is the effective crosstalk capacitance, R_{victim} is the wire resistance of the victim line and $t_{aggressor}$ is the switching slew rate of the aggressor line.

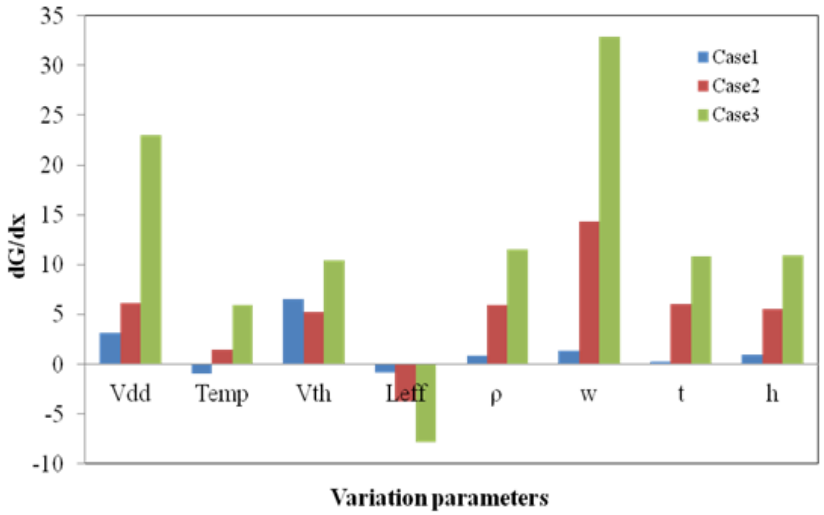

Figure 7: Crosstalk glitch sensitivity to variability of a minimally spaced wire with no buffer

The next step is to investigate the impact of buffer insertion and wire spacing on crosstalk glitch sensitivity to variation parameters. The same linear model is used for the crosstalk glitch of Case 2 with the same interconnect geometry but with $s = 3wmin$ for wire spacing analysis, and $s = wmin$ with 3 buffers for buffer insertion analysis. A comparison of the results is shown in Figure 8. The decrease in the crosstalk glitch sensitivity is more significant through the wire spacing method as it is known to be the most effective way in reducing crosstalk noise. Increasing the distance between the adjacent wires will result in reduction of crosstalk capacitance and thus the crosstalk glitch. With buffer insertion, the crosstalk glitch sensitivity to the wire parameter variations is reduced but there is a slight increase in dependency towards the device parameter variations. This is due to the use of buffers which contribute to the increase in the crosstalk glitch dependency of *Leff*, which is contributed by the driving capability of the low-swing driver and buffers.

For cases 2 and 3 second order models for the crosstalk glitch on the middle line in Figure 3 were generated using Minitab to observe the interaction and quadratic effects on the crosstalk glitch

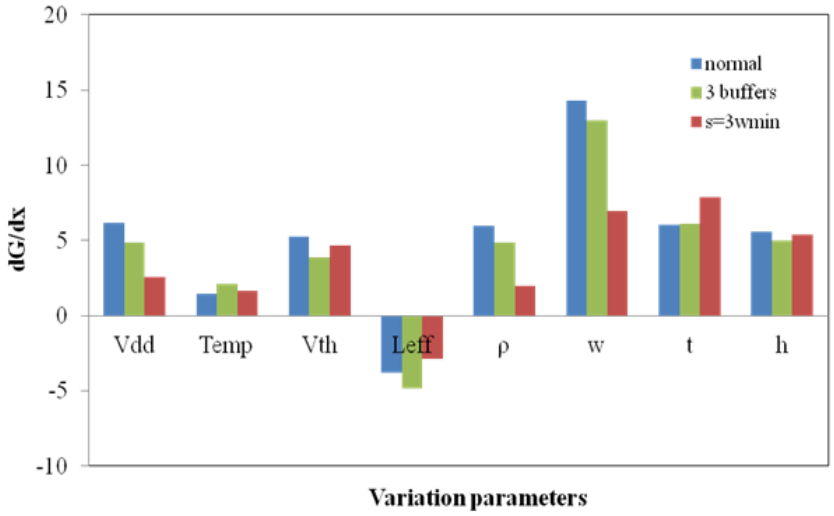

Figure 8: The impact of wire spacing and buffer insertion on crosstalk glitch sensitivity to variability

variations. The accuracy of these models was validated using R^2 fit analysis which was found to be more than 99% for all cases. For this analysis, a 10 mm minimally spaced wire with no repeaters was considered. The results are as shown in Table 4. The coefficients stated in Table 4 represents the regression coefficients (β) for each variation parameters, which in this case are the interaction and quadratic effects of the process parameters.

A comparison was made between the second order models and the linear models shown in Figure 7. The comparison clearly indicates that the linear coefficients are more significant or more specifically the linear coefficient of *Vdd*, ρ and *h*. The non-linear effects can totally be ignored as they will not have a significant impact on the model accuracy. However, some of the non-linear effects especially for Case 3, show that it can contribute to the model but with them correlating with *Vdd*, it can be assumed that the sole effect of *Vdd* is already enough to have a significant impact on the model accuracy.

5. CONCLUSION

An analysis was carried out to investigate the impact of variability on crosstalk effects of the low-swing signalling schemes. Both first and second order models were generated for crosstalk delay and noise. The results indicate that the delay and glitch sensitivities have a high data dependency towards *Vdd* and wire parameter variations. This dependency can be reduced through buffer insertion and wire spacing with the latter method being the most effective difference in delay whilst wire spacing is found to be the most effective method in reducing variability in crosstalk noise. Results from the second order model indicate that most of the non-linear effects can be ignored as they are insignificant to provide an impact on the model accuracy. However, a few coefficients such as the quadratic effects of *Vth*, *w* and *h* and the interaction between *Vdd* and ρ should be considered as they can be regarded as significant to the crosstalk delay sensitivity compared to the linear coefficients.

In this variability analysis on the crosstalk effects, the most significant variables as well as their interactions and quadratic coefficients have been identified which aids in distinguishing the right process choice on whether the response of interest is crosstalk delay or glitch. Subsequently, statistical models which represent the crosstalk delay and noise with the interactions of the

Table 4: Interaction coefficients of device, interconnect and environmental variations

	Case 2	Case 3		Case 2	Case 3
Vdd^2	2.2	5.2	ρ^2	3	3.2
$Temp^2$	1.8	3.4	w^2	0.8	0.1
Vth^2	1.9	3.3	t^2	0.6	0.5
$Leff^2$	0.2	1.2	h^2	-4	-10
$Vdd*Temp$	1.5	2.9	$\rho*w$	-3.6	1
$Vdd*Vth$	-0.8	-3.9	$\rho*t$	-0.1	0.2
$Vdd*Leff$	-0.4	0.9	$\rho*h$	0.1	-0.2
$Temp*Vth$	0.1	-2	$w*t$	0.3	0.1
$Temp*Leff$	0.05	1	$w*h$	-0.2	-0.8
$Vth*Leff$	-0.5	0.1	$t*h$	0.4	-0.1
$Vth*\rho$	-2.4	-0.7	$Vdd*\rho$	-0.9	-2.4
$Vth*w$	2	0.4	$Vdd*w$	1.9	4.8
$Vth*t$	-0.1	0.3	$Vdd*t$	-0.5	1.4
$Vth*h$	-0.4	0.5	$Vdd*h$	-0.4	1.3
$Leff*\rho$	-0.5	0.2	$Temp*\rho$	-0.9	0.3
$Leff*w$	0.3	0.45	$Temp*w$	1.5	0.7
$Leff*t$	1.3	0.4	$Temp*t$	-0.6	0.5
$Leff*h$	0.9	0.3	$Temp*h$	-0.8	0.4

significant parameter variations were developed which can be incorporated into any low-swing signalling scheme to find the best results in reducing the crosstalk effects in the variability environment.

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