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Design, Analysis and Comparisons of the 0.18 μm CMOS W-CDMA PCSNIM LNA with Common Drain and Class AB Buffers

Norlaili Mohd Noh, Tun Zainal Azni Zulkifli, Wong Pi Wei, Chow Wei Sheng

Advanced Integrated System Device (AISDe) Group,
School of Electrical and Electronic Engineering,
Universiti Sains Malaysia, Engineering Campus
14300 Nibong Tebal, Pulau Pinang, Malaysia

Tel: +604-5996023, Fax: +604-5941023, E-mail: eelaili@eng.usm.my

Abstract—Buffers are used to provide output impedance transformation for the cascode low noise amplifiers (LNAs). However, the issue is always with the large current consumption that may be required by the buffer circuits. In the search to obtain an efficient buffer design that can simultaneously fulfill the output matching and application requirements of an LNA, the performance of an LNA with the typical common drain (CD) and Class AB voltage follower circuits are analyzed and compared. The application is for a W-CDMA receiver with the LNA being of the power-constrained simultaneous noise and input matching(PCSNIM) type. Using Silterra's 0.18 μm RFCMOS 6-metal-1-poly process, the results show that for providing a 50 Ω impedance match, both buffer designs provide similar performance and are applicable for the W-CDMA application. PCSNIM LNAs with a total current consumption of not more than 5.6 mA, power gain of not less than 17.6 dB, reverse isolation of better than -40 dB, NF of not more than 2.1 dB and a power consumption of about 10 mW are able to be obtained. The PCSNIM with Class AB voltage follower is superior in terms of consuming 0.6 mA less of current and consequently, 1.1 mW less of power. However, it is lacking in other performance metrics; linearity (3rd-order input intercept point, IIP3) worse by 6.5 dBm, power gain (S21) less by 2 dB, and noise figure (NF) is more by 0.4 dB.

Keywords: CMOS output buffer, common-drain, class AB voltage follower, PCSNIM LNA, W-CDMA.

1. INTRODUCTION

A buffer circuit is especially important if there exists a mismatch between the output impedance of the amplifier and the impedance of the load. For a cascode LNA, the high output impedance possessed by this topology and the typical 50 Ω requirement of the load makes the buffer circuit indispensable.

The inductively-degenerated cascode (IDC) is a typical configuration of the LNA as it provides simultaneous noise and input matching and very good reverse isolation performance, especially important for the W-CDMA front-end design. An additional capacitor placed across the input transistor of the IDC LNA distinguishes the PCSNIM LNA from the typical IDC LNA. The schematic of such a topology and the corresponding small signal model are shown in Figure 1.

The buffer circuits designed, analyzed and compared in this work are of the CD and Class AB types. Each buffer type is constructed at the output of the PCSNIM LNA. The size of the transistors used in the PCSNIM LNAs was determined using the power-constrained noise optimization (PCNO)

method. The design of the LNAs with buffer were performed using Silterra's 0.18 μm CMOS process. The values of the components in the schematic are shown in Table 1.

The paper starts with a short introduction, followed by the analysis of the circuits and methodology in designing the PCSNIM LNA, the CD and the Class AB buffers. The results of the simulation performed on these circuits to determine their abilities in conforming to the W-CDMA requirements are then presented and discussed. Subsequently, conclusions are given on the capabilities of each buffer circuit and their ability to work in a W-CDMA application. The paper ends with the acknowledgements to the parties involved and a reference list constituting the references used in completing this paper.

Table 1: Components and parameters values for PCSNIM, PCSNIM with CD buffer and PCSNIM with Class AB buffer. "na" means not applicable

Parameter/ Component	PCSNIM	PCSNIM with CD buffer	PCSNIM with Class AB buffer
f_o (GHz)	2.14		
V_{DD} (V)	1.8		
L (μm)	0.18		
R_S (Ω)	50		
R_1, R_2(kΩ)	9, 2.5		
R_{ref1} (kΩ)	na		4
R_{b1} (kΩ)	na		0.3
R_{b2} (kΩ)	na		0.15
C_c (pF)	75		
C_d (pF)	0.35		0.1
C_{c1} (pF)	75	10	3.6
C_{ex} (pF)	0.32	0.1	0.5
C_o (pF)	na	0.13	na
C_{bat} (pF)	na		0.5
L_g (nH)	7.66	6.94	7.66
R_o (kΩ)	na	2.5	na
L_d (nH)	15.8	15.8	4.21
L_s (nH)	0.55		
M_1 (μm/μm)	290/0.18		
M_2 (μm/μm)	290/0.18	145/0.18	
M_3 (μm/μm)	20/0.36		
M_4 (μm/μm)	na	100/0/18	na
M_5 (μm/μm)	na	100/0.18	na
M_{ref1} (μm/μm)	na		38.4/0.72
M_{ref2} (μm/μm)	na		38.4/0.72
M_{buf1} (μm/μm)	na		76.8/0.18
M_{buf2} (μm/μm)	na		76.8/0.18
M_{RL} (μm/μm)	na		20.5/0.18

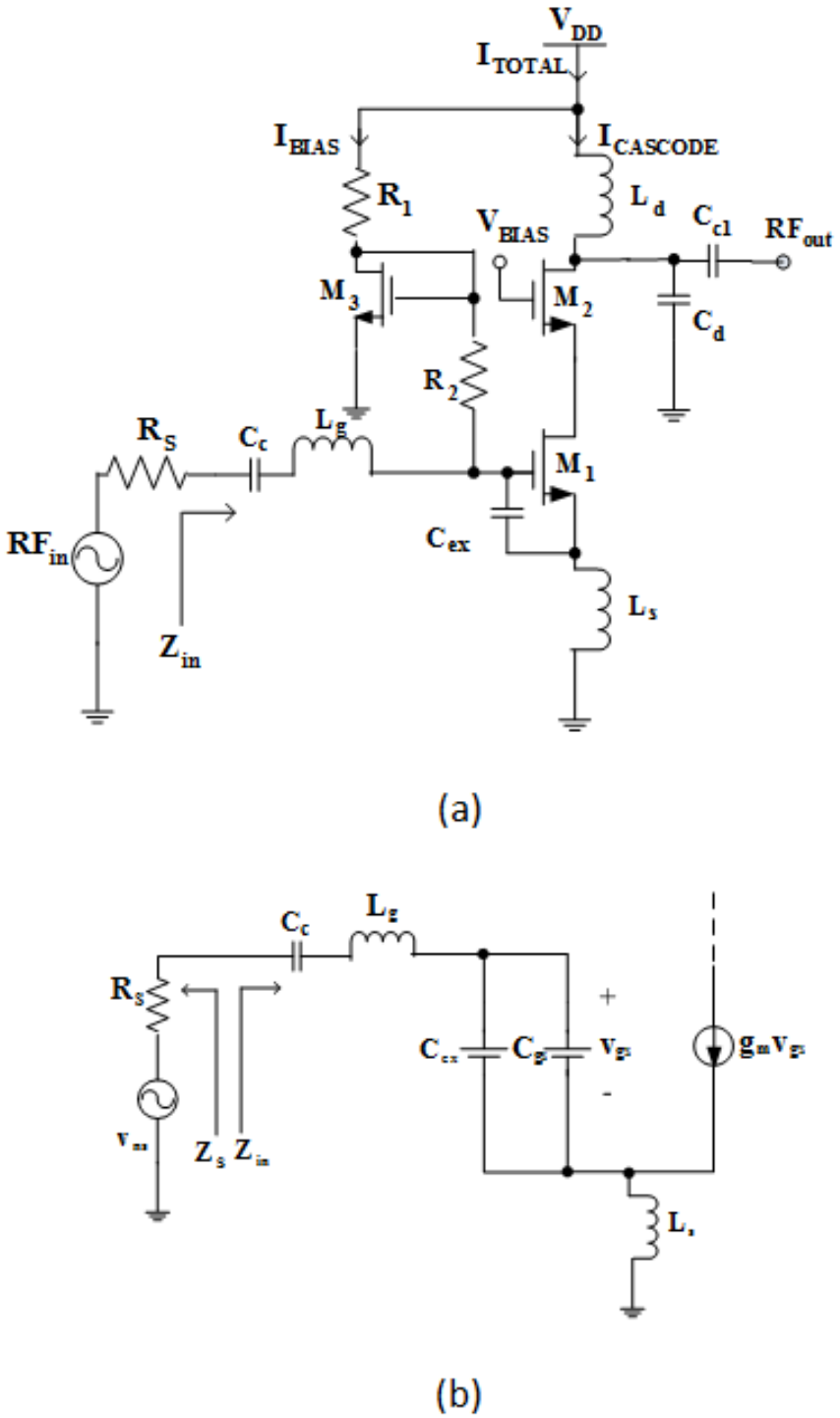

Figure 1: The PCSNIM LNA [1],[2]: (a)Schematic; (b)Small-signal model of the input stage

2. THE PCSNIM LNA DESIGN METHODOLOGY

As the buffer is to be placed at the output of the PCSNIM LNA, this section will present the design methodology of this LNA. The LNA was designed for the operating frequency of 2.14 GHz, which is the center frequency of the reception range (2.11 to 2.17 GHz) of a W-CDMA receiver. A flowchart of the design methodology of the mentioned LNA is given in Figure 2.

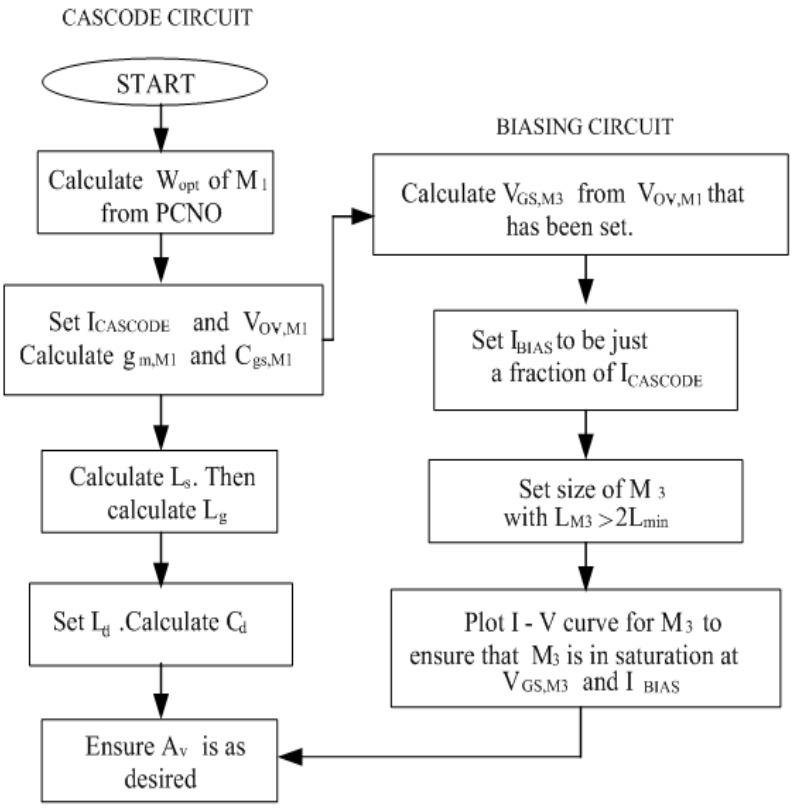

Figure 2: A Flowchart on the Design Methodology of the PCSNIM LNA [1]

Referring to Figure 2, W_{opt} is the optimum width of the input transistor, M_1. $I_{CASCODE}$ is the current that is flowing through M_1 and M_2 in the cascode circuit. $V_{0V,M1}$ is the overdrive voltage of M_1, $g_{m,M1}$ is the transconductance of M_1, $C_{gs,M1}$ is the gate-to-source voltage of M_1, $V_{GS,M3}$ is the gate-to-source voltage of M_3. I_{BIAS} is the current that is flowing through M_3 which is the transistor in the biasing circuit. Av is the voltage gain. L_{M3} and L_{min} are the length of M_3 and minimum length of device, respectively.

2.1. Transistor Size

The design starts with the determination of W_{opt} by using the PCNO technique. Optimum width means the width of the input transistor that can provide the circuit input impedance to be very close to the value of the noise input impedance. The equation used to determine W_{opt} is as follows [1],[2]:

$$W_{opt} = \frac{3}{2\omega_0 L C_{ox} Q_{s,opt} R_s} \tag{1}$$

where ω_0 is $2\pi(2.14 \times 10^9)$ rad/s, length L is 0.18 μm, C_{ox} is oxide capacitance of the transistor, $Q_{s,opt}$ is 4.5 [1],[2] and R_s is the source resistance and typically set as 50 Ω. In this work, W_{opt} is calculated to be approximately 290 μm.

2.2. Passive Components

2.2.1. Input Stage

Referring to Figure 1(b),

$$Z_{in} = s(L_g + L_s) + \frac{1}{(sC_T)} + (\frac{g_{m,M1}L_s}{C_T}) \tag{2}$$

where C_T is the sum of the gate-source capacitance of M_1, $C_{gs,M1}$, and C_{ex}. $C_{gs,M1}$ is calculated to be 0.33 pF when W is equivalent to W_{opt}. At resonance, Z_{in} is 50 Ω and

$$Z_{in} = \frac{g_{m,M1}L_s}{C_T} \tag{3}$$

$$g_{m,M1} = \mu C_{ox}(W/L)_{M1}V_{0V,M1} \tag{4}$$

From (4), $g_{m,M1}$ is calculated to be 59 mS when $V_{0V,M1}$ is 0.1 V. The minimum possible inductor for the Silterra 0.18 μm process is 0.55 nH [1]. Therefore, C_T is calculated to be 0.65 pF. Hence, C_{ex} is 0.32 pF. Also at resonance [1],

$$L_g = \left[\frac{1}{\omega^2 C_T}\right] - L_s \tag{5}$$

L_g is calculated to be about 8 nH. The inductance closest to this value available with the process is 7.66 nH.

2.2.2. Output Stage

Since the L_d is required to resonate with the C_d to tune the output signal to 2.14 GHz, their relationship is expressed by

$$\omega_0^2 = \frac{1}{L_d C_d} \tag{6}$$

Setting L_d to be 15.8 nH, C_d is 0.35 pF.

2.3. The Biasing Circuit

Typical current in a W-CDMA single-ended 0.18 μm CMOS LNA is in the vicinity of 4 mA to 4.5 mA to give a gain of 9 dB to 18 dB [3],[4]. For this purpose, the M_1 with a gate-to-source voltage, V_{GS}, in the range of 0.6 V to 0.63 V will be appropriate [1]. The current consumed by the amplifying transistor will be about 3 mA (from the general equation $I_D = (\mu C_{ox}/2)(W/L)V_{ov}^2$) [1],[2]) and only a small fraction of this needs to be reserved for the current consumed by the on-chip biasing circuitry. If the width of M_3 is set to 10 μm, then the current that will be flowing is 100 μA at the transistor's minimum length. To have a more reliable biasing performance, the length of M_3 is made twice of its minimum and the width will become 20 μm if the same current is desired. Hence, the total current ($I_{TOTAL} = I_{CASCODE} + I_{BIAS}$) will not be more than the one estimated. Since M_3 and M_1 form a current mirror, they are related by the following equation,

$$\frac{W_{M1}/L_{M1}}{W_{M3}/L_{M3}} = \frac{I_{D,M1}}{I_{D,M3}} \tag{7}$$

where W_{M1} and L_{M1} are the width and length of M_1, respectively, and W_{M3} and L_{M3} are the width and length of M_3, respectively. From (7) and using the values stated above, $I_{D,M1}$ is calculated to be 2.9 mA. On the other hand, if $I_{D,M1}$ is 4 mA, then $I_{D,M3}$ will be almost 140 μA. Looking at Figure 1(a), $I_{D,M1}$ is $I_{CASCODE}$ and $I_{D,M3}$ is I_{BIAS}.

When the $V_{GS,M1}$ is 0.6 V, the $V_{DS,M3}$ is also at the same voltage. Since the supply voltage is 1.8 V, R_1 is 12 kΩ or almost 9 kΩ for $I_{D,M1}$ of 3 mA or 4 mA, respectively. In this work, R_1 used is 9 kΩ and the resultant $I_{D,M1}$ is expected to be close to 4 mA. R_2 is a large resistance that will prevent noise from the supply from entering the LNA. A resistor in kΩ will be sufficient [2] and in this work, R_2 is chosen to be 2.5 kΩ.

3. THE BUFFER DESIGNS

Two buffer designs are presented in this paper. The first is the basic CD circuit and the second is the Class AB voltage follower. Figure 3(a) and 3(b) show the CD and Class AB voltage follower circuits, respectively. In both circuits, C_{C1} is the coupling capacitor that will isolate the biasing of the buffer from the LNA circuit. The C_C at the drain of M_2 in Figure 1(a) is replaced by C_{C1} for the circuits in Figure 3.

3.1. The CD Buffer

Referring to Figure 3(a), M_4 is operating as the voltage buffer and M_5 is the current source. L_d and C_d (from Figure 1(a)), gate-to-source capacitance of M_4, $C_{gs,M4}$, C_0 and gate-to-drain capacitance of M_5, $C_{gd,M5}$ (from Figure 3(a)) will tune the output signal to 2.14 GHz. R_0 has the same function as R_2 in Figure 1(a).

The output resistance of the CD transistor M_4 is $1/g_{m,M4}$, where $g_{m,M4}$ is the transconductance of M_4. To transform the output impedance of the cascode to 50 Ω, the output resistance of M_4 should be 50 Ω. Hence, $g_{m,M4} = 0.02$ S. From Equation (4), the widths of M_4 and M_5 can be obtained; i.e. $W_{M4} = W_{M5} \approx 100$ μm at $V_{0V} = 0.1$ V. Expected current to flow, $I_{D,M4} = I_{D,M5}$ is ≈ 1 mA. So, the total current flowing through the IDC LNA, the biasing circuit and the CD buffer is estimated to be around 5 mA.

In determining the output impedance, Z_{out}, of the PCSNIM LNA with CD buffer, Figure 4 is referred to. $Z_{out,cascode}$ is the output impedance of the cascode. The large coupling capacitor, C_{C1}, can be assumed to be a short-circuit and the 2.5 kΩ can be assumed to be an open-circuit at the operating frequency. In determining the output impedance of the buffer, input v_{i,CD_buffer} is shorted to ground. Hence, v_{gs4} is also the voltage drop across the dependent current source $g_{m4}v_{gs4}$. Therefore, the dependent current source can be represented by a $1/g_{m4}$ resistance, which in this case is 50 Ω. Since this resistor is in parallel with r_{o5} and the latter is a much larger resistance, r_{o5} can be ignored.

Referring to Table 1, the width of M_2 is half of the width of M_1 for the PCSNIM LNA with CD buffer. This is to accomplish a better input 3rd order intercept point, IIP3, based on the study by [5]. It was shown in this paper that M_2 has more influence on the linearity performance of the cascode as compared to M_1. If the linearity of the LNA needs to be optimized, modifications should be performed on M_2. To reduce the effect of the series resistance of L_g on the NF of the PCSNIM LNA with CD buffer, the L_g chosen is less than the one for PCSNIM LNA without buffer (refer to Table 1).

Looking at Figures 3(a) and 4, the CD has some limitations in terms of the current and output voltage swing are highly dependent on V_{GS4}. In addition, Figure 4 shows that the output impedance is greatly affected by $1/g_{m4}$ and in order to reduce the output impedance, g_{m4} needs to be increased resulting in higher current consumption by the buffer circuit. To overcome the limitations of the CD buffer, a Class AB voltage follower was designed based on [6]. This circuit is able to improve the output voltage swing and enhance the bandwidth [6].

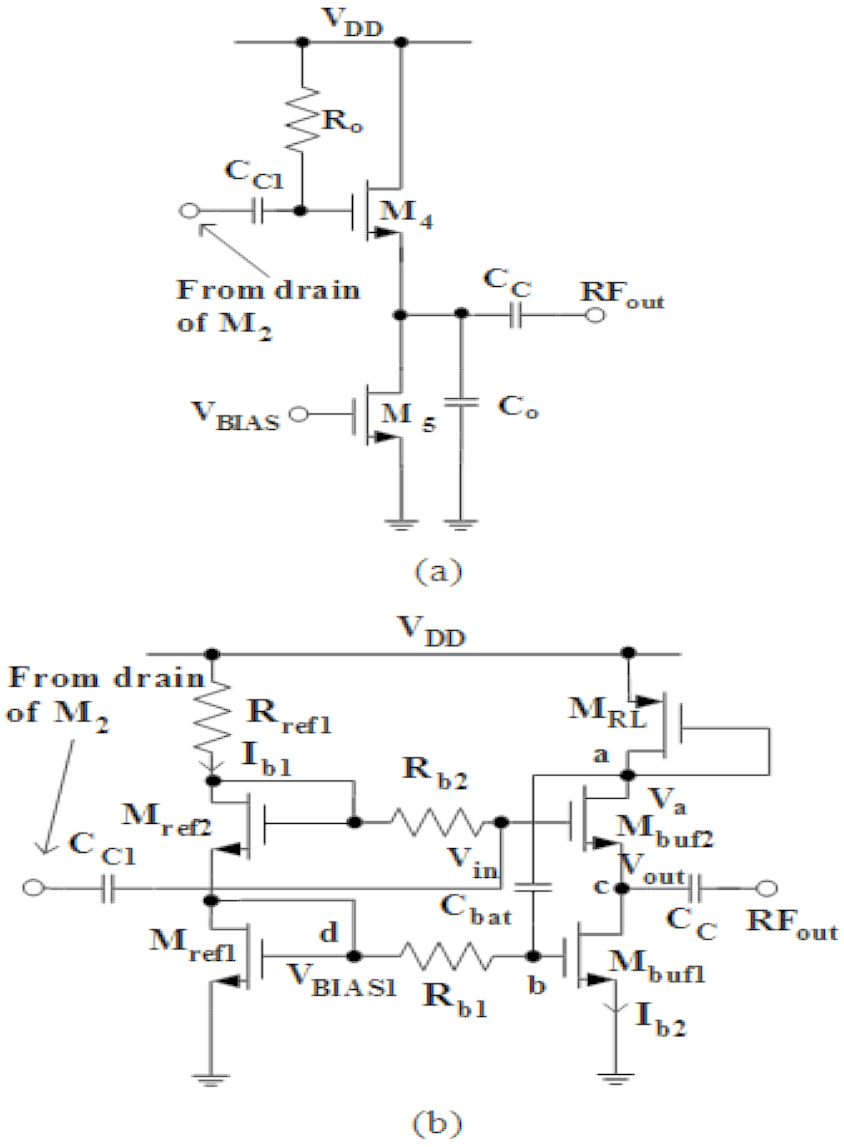

Figure 3: The buffer schematics: (a)The CD; (b)The Class AB voltage follower

3.2. The Class AB Voltage Follower

This circuit is based on the quasi-floating gate (QFG) technique which utilizes a large resistive element to set the quiescent voltage at the gate of the transistor which is known as the QFG node [6]. This node has a well defined quiescent voltage but it performs as a floating node under ac condition [6].

Referring to Figure 3(b), R_{b1} is used to set the gate of the biasing transistor M_{buf1} to a quiescent voltage of V_{BIAS1}. M_{RL} is diode connected and represents the load resistor, R_L, that provides the node 'a' a voltage V_a which is inverted but approximately the same magnitude as the input voltage V_{in}. A PMOS was chosen to avoid the body effect. R_L is $1/g_{m,M_{RL}}$. Under dynamic conditions, there is a fast change in V_{in} whereas V_{out} is slewing, the output node 'c' will momentarily be a signal ground [6]. Under these conditions, M_{buf1} together with R_L operate as a common source amplifier

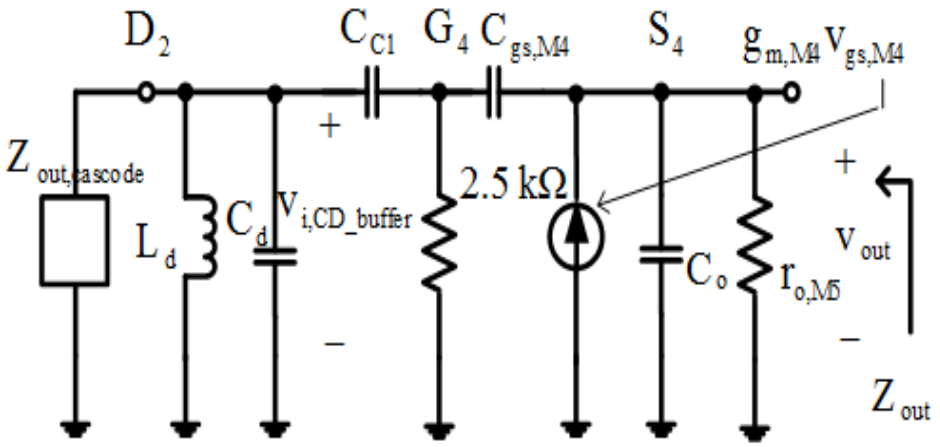

Figure 4: The small-signal model of the CD buffer stage

with a gain of $A_v = V_a/V_{in} = -g_m R_L$ [6]. Capacitor C_{bat} performs as a floating battery due to the fact that it cannot acquire rapidly the charge on node 'a' because of the large time constant $\tau = R_{b1}C_{bat}$. Hence the voltage variations at node 'a' are transferred to node 'b' [6].

When V_{in} increases, V_a and V_b decrease which results in the current through M_{buf1} being reduced. The current reduction in M_{buf1} leads to the decrement of V_{out} and the increment of the gate-source voltage of M_{buf2}, $V_{GS,Mbuf2}$. Consequently, large positive current flows through C_L. On the other hand, when V_{in} decreases, V_a and V_b increase and the current in M_{buf1} increases. This causes a large negative output current in C_L. This is how class-AB voltage follower operates and it is effective starting at the corner frequency, $\omega_c = 1/(R_{b1}C_{bat})$ [6].

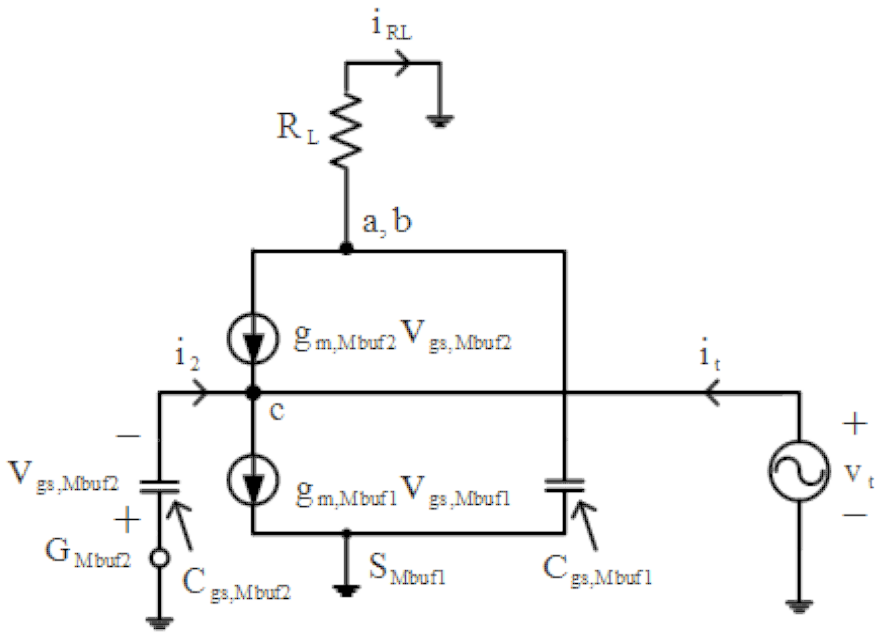

Figure 5: The small-signal model of the Class AB buffer when determining Z_{out}

At higher frequencies, it can be assumed that there is a short-circuit between node a and b (referring to Figure 3(b)). If the impedance at the output is large, M_{buf1} and M_{buf2} form a negative feedback loop with an open-loop gain given by $g_{m,Mbuf1}R_L$ [6]. Figure 5 shows the small-signal model of the Class AB buffer under this condition. Referring to Figure 5, the output impedance is [6]:

$$Z_{out} = \frac{V_t}{i_t} = \frac{1}{\frac{g_{m,Mbuf1}g_{m,Mbuf2}}{\frac{1}{R_L}+sC_{gs,Mbuf1}} + g_{m,Mbuf2} + sC_{gs,Mbuf2}} \tag{8}$$

For small transistors,

$$Z_{out} \approx \frac{1}{g_{m,Mbuf1}g_{m,Mbuf2}R_L} = \frac{g_{m,MRL}}{g_{m,Mbuf1}g_{m,Mbuf2}} \tag{9}$$

To design the circuit in Figure 3(b):

$$R_{ref1} = \frac{V_{DD} - (V_{0V,Mref2} + V_{th,Mref2}) - V_{DS,Mref1}}{I_{b1}} \tag{10}$$

$V_{OV,Mref2}$ and $V_{th,Mref2}$ are the overdrive and threshold voltages of M_{ref2}, respectively. $V_{DS,Mref1}$ is the drain-source voltage of M_{ref1}. Since M_{ref1} and M_{buf1} form a current mirror, then

$$I_{b2} = \left[\frac{(W/L)_{Mbuf1}}{(W/L)_{Mref1}}\right] I_{b1} \tag{11}$$

$$\frac{(W/L)_{Mbuf2}}{(W/L)_{Mref2}} = \frac{(W/L)_{Mbuf1}}{(W/L)_{Mref1}} \tag{12}$$

From Figure 3(b),

$$V_{GS,Mref2} + V_d = V_{GS,Mbuf2} + V_c \tag{13}$$

Equation (13) indicates that $V_{gs,Mref2} = V_{gs,Mbuf2}$ and $V_d = V_c$ if $I_{b1} = I_{b2}$ and $(W/L)_{Mref2} = (W/L)_{Mbuf2}$. This condition maintains although M_{ref2} and M_{buf2} suffer from body effect [7]. This is the advantage of using a cascode current mirror which enables better current copying capability. R_{b1} is used to set the gate of the biasing transistor M_{buf1} to a quiescent voltage of V_{BIAS1}. R_{b2} is used to set quiescent voltage of the input which is the voltage of the gate of M_{buf2}.

Designing the Class AB buffer starts with setting the current consumed by the total buffer circuit to be about 1 mA. This is to ensure that the whole LNA with buffer circuit will consume around 5 mA of current, as targeted. Setting $I_{b2}/I_{b1} = 8$ so that the biasing circuitry of the buffer consumes just a small fraction of the total current of the buffer, I_{b2} is calculated to be 0.88 mA and I_{b1} is 0.11 mA. With the mentioned amount of current flowing through M_{buf1} and M_{buf2} and setting $V_{0v,Mbuf1} = V_{0v,Mbuf2} = 0.1$ V, then $W_{Mbuf1} = W_{Mbuf2} = 86$ μm at minimum length.

Subsequently, $W_{Mref1} = W_{Mref2} = 43$ μm at an overdrive voltage of 0.1 V and length of 0.72 μm. A larger length is required to enable a more stable biasing performance. From the width and length of M_{buf1}, M_{buf2}, M_{ref1} and M_{ref2}, Equations (11) and (12) are justified. $V_{GS,Mbuf1} = V_b = V_a = V_{SG,MRL} = V_{SD,MRL} \approx 0.5$ V. $V_{0v,MRL} \approx 0.9$ V. From calculation, $W_{MRL} \approx 4.2$ μm.

Since $V_{0v,Mref1} = V_{0v,Mref2} = 0.1$ V, then $V_{DS,Mref1} = V_{DS,Mref2} = 0.515$ V. Hence, R_{ref1} is about 7 kΩ from [1.8 - 2(0.515)] V/0.11 mA. f_c of the R_{b1} and C_{bat} high-pass filter is set to 1/2 of 2.14 GHz to ensure that the W-CDMA downlink frequency range of 2110 MHz to 2170 can be obtained at the output. Setting C_{bat} as 500 fF, R_{b1} was calculated to be 300 Ω.

Optimized performance of the PCSNIM LNA with the Class AB buffer was achieved when the components and devices were at the values as shown in Table 1. Reduced W_{Mref1}, W_{Mref2},

W_{Mbuf1} and W_{Mbuf2} result in an overall lower current consumption. The much reduced R_{ref1} indicates that the pre-assumed $V_{0V,Mref1} = V_{0V,Mref2} = 0.1$ V may not be the value to provide the best performance. With this optimized design, the mentioned LNA was able to achieve the targeted performance following the W-CDMA specifications as shown in Table 2.

4. RESULTS AND DISCUSSION

The S-parameters and NF performances were obtained from simulation performed on the PCSNIM LNA shown in Figure 1(a) and with CD and Class AB buffers shown in Figure 3(a) and (b), respectively. The component and parameter values are given in Table 1.

It is seen from Figure 6 that the PCSNIM LNA with the CD buffer is input matched to 2.53 GHz rather than the desired 2.14 GHz. The reason for this display of performance is due to the mistake of using a C_T of 0.43 pF. Using Equation (5), $f_o = 2.8$ GHz at this capacitance. Hence, the C_T that should have been used is 0.74 pF. Consequently, the C_{ex} that can tune the input stage to the desired frequency is 0.41 pF. For the PCSNIM LNA with the Class AB buffer, the result verifies Equation (5).

The S_{22} performance of the PCSNIM LNA indicates the importance of implementing the buffer circuit. Without the buffer circuit, it is impossible for the output stage of this LNA to be matched to the 50 Ω load. This is due to the high output impedance of the cascade. The S_{22} achieved at 2.14 GHz was a mere -0.7 dB. Figure 7 shows that the S_{22} performances of the PCSNIM LNAs with buffer are following the requirement of the W-CDMA. The S_{22} is about -21 dB at 2.12 GHz for the PCSNIM LNA with the AB follower whereas the PCSNIM LNA with CD buffer is tuned to 2.17 GHz.

S_{21} performances are also good with power gain of more than 18 dB for the PCSNIM LNAs with buffer. The results are shown in Figure 8. The PCSNIM LNA with the CD buffer is superior by about 2 dB at the frequency of interest. For the PCSNIM LNA without buffer, the result shows that the S_{21} obtained is only about 10 dB at 2.14 GHz and the LNA is actually tuned to 1 to 1.5 GHz at a power gain of about 12.5 dB. This of course is due to the unmatched output stage. This finding also indicates that gain is more influenced by the output stage, rather than the input, as the mentioned LNA displays good S_{11} result shown by the previous figure.

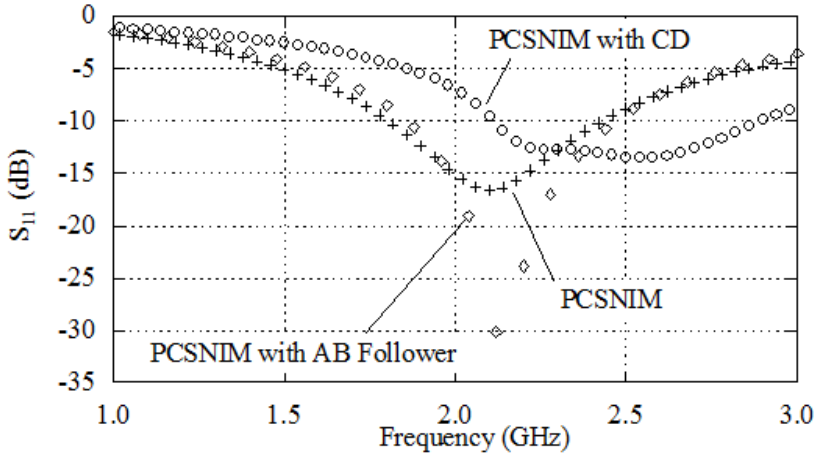

Figure 6: The S_{11} performance

Figure 9 shows that the S_{12} of the LNA is greater influenced by the S_{22} and less by the S_{11}. Although the PCSNIM LNA with the CD buffer is not input matched at 2.14 GHz, its S_{12} is still

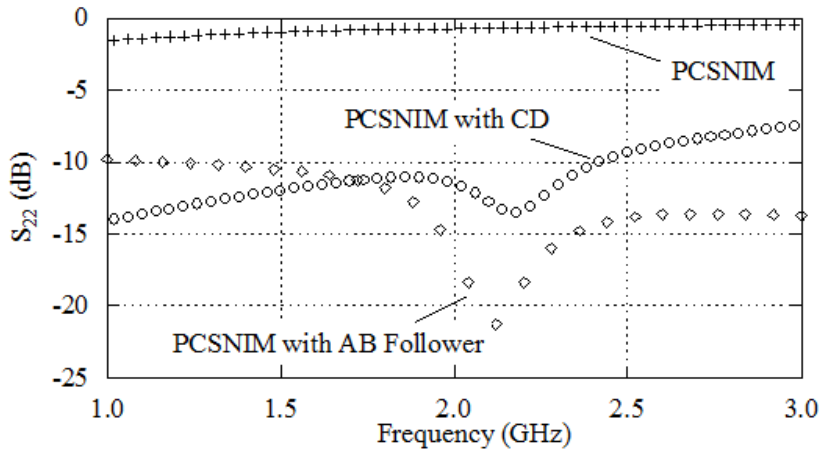

Figure 7: The S_{22} performance

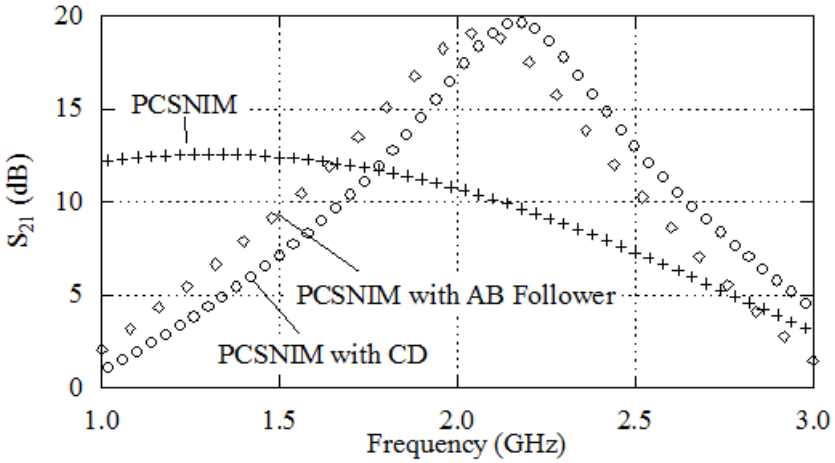

Figure 8: The S_{21} performance

tuned to the desired frequency due to its matched output. The S_{12} of not lower than |40 dB| indicates that the cascode with buffer topologies are able to provide very good output to input isolation.

Finally, the NF performances of all LNA circuits shown in Figure 10 confirm that all circuits are able to abide to the noise requirement set by the W-CDMA. At 2.14 GHz, all circuits display NF of less than 2.5 dB. The performances of all PCSNIM LNAs are summarized in Table 2. Table 2 also shows that the gain superiority (by 2 dB) of the PCSNIM LNA with CD buffer is at the expense of a higher current consumption (by 0.6 mA). However, it also displays better linearity (IIP_3 - by 6.5 dBm) and noise (NF - by 0.4 dB) performances.

Since the work was motivated by the issue of buffer circuits in LNAs consuming significant amount of current, it is appropriate to mention here that the current consumed by the CD buffer is about 28.6% of the total LNA with CD buffer current whereas the Class AB buffer consumes only 20% of the total current flowing through the LNA with Class AB buffer. However, in general, the performance of both circuits can be said to be equivalent for W-CDMA application.

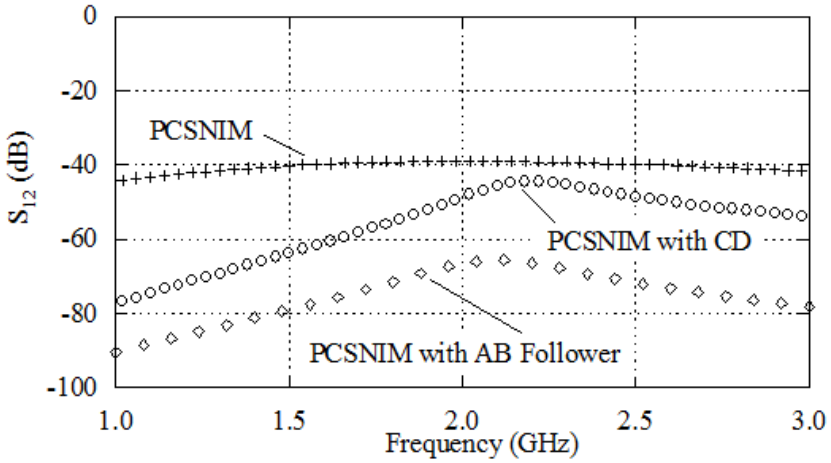

Figure 9: The S_{12} performance

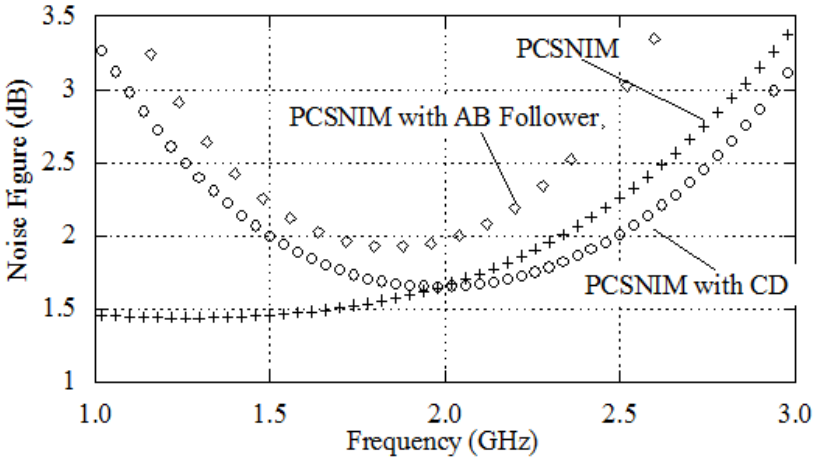

Figure 10: The NF performance

To measure the capability of the LNAs designed, the performance of these circuits were benchmarked against similar work by others. Table 3 summarizes the performances of a few similar LNAs with buffer, designed by others. These work by others are not operating under exactly the same conditions as our work, but nevertheless, comparison can still be made to perform a general benchmark.

Referring to Table 3 and work by [11], [12] and [13] which were all performed using the 180 nm technology, power gain of this work is at par with the one obtained by [11] and much better than work by [12] and [13]. However, the result shown by [12] is from measurement.

Power consumed by the LNAs in this work is less than consumed by the LNAs from the work by [11] to [13]. But the designs by [11] to [13] were operated at higher frequencies and again, [12] provides measured results. The NF obtained in this work is also better than achieved by [11] to [13]. However, their circuits are working at slightly higher frequencies.

In general, it can be concluded that the results from this work for both PCSNIM LNA with CD and Class AB buffers are comparable with similar LNA designs by others. Figure 11 shows the

Table 2: Results at 2.14 GHz from post-layout simulation. "na" is not applicable

Metrics	W-CDMA Specs. [8]	PCSNIM [1]	PCSNIM LNA with CD buffer [1]	PCSNIM LNA with Class AB buffer (this work)
S_{11} (dB)	<-10	-16.4	-10.9	-16.4
S_{12} (dB)	<-30	-39	-44.8	-67.2
S_{21} (dB)	>15	9.9	19.6	17.6
S_{22} (dB)	<-10	-0.7	-13.36	-24.4
NF (dB)	<2.5	1.8	1.7	2.1
IIP_3 (dBm)	>-15	1.3	-9.9	-16.4
I_{buffer} (mA)	na	na	1.6	1
I_{total} (mA)	na	4.0	5.6	5.0
Power (mW)	na	7.2	10.1	9.0

layouts of the three LNA configurations discussed in this paper.

5. CONCLUSION

The PCSNIM LNA with the typical CD buffer and Class AB voltage follower had been successfully designed. Detailed analysis of the circuits and design methodology had been shown. The PCSNIM LNA with Class AB voltage follower was implementing the buffer designed by Ramirez-Angulo et al.[6]. Comparisons were made and the results showed that both PCSNIM LNA with CD buffer and PCSNIM LNA with Class AB voltage follower gave similar performances. Both buffers can be utilized to fulfill the requirements for W-CDMA applications. Nevertheless, the PCSNIM LNA with CD buffer shows superiority in almost all performance metrics - power gain, NF and IIP_3. It lacks only in terms of current and power consumption. In addition, the layout size of the Class AB buffer is also larger than the CD due to the extra 3 transistors and 2 resistors.

A PCSNIM without buffer was also designed and performance was compared with the other two LNAs to show the importance of implementing the buffer circuits in cascode LNAs in the matching of the output stage.

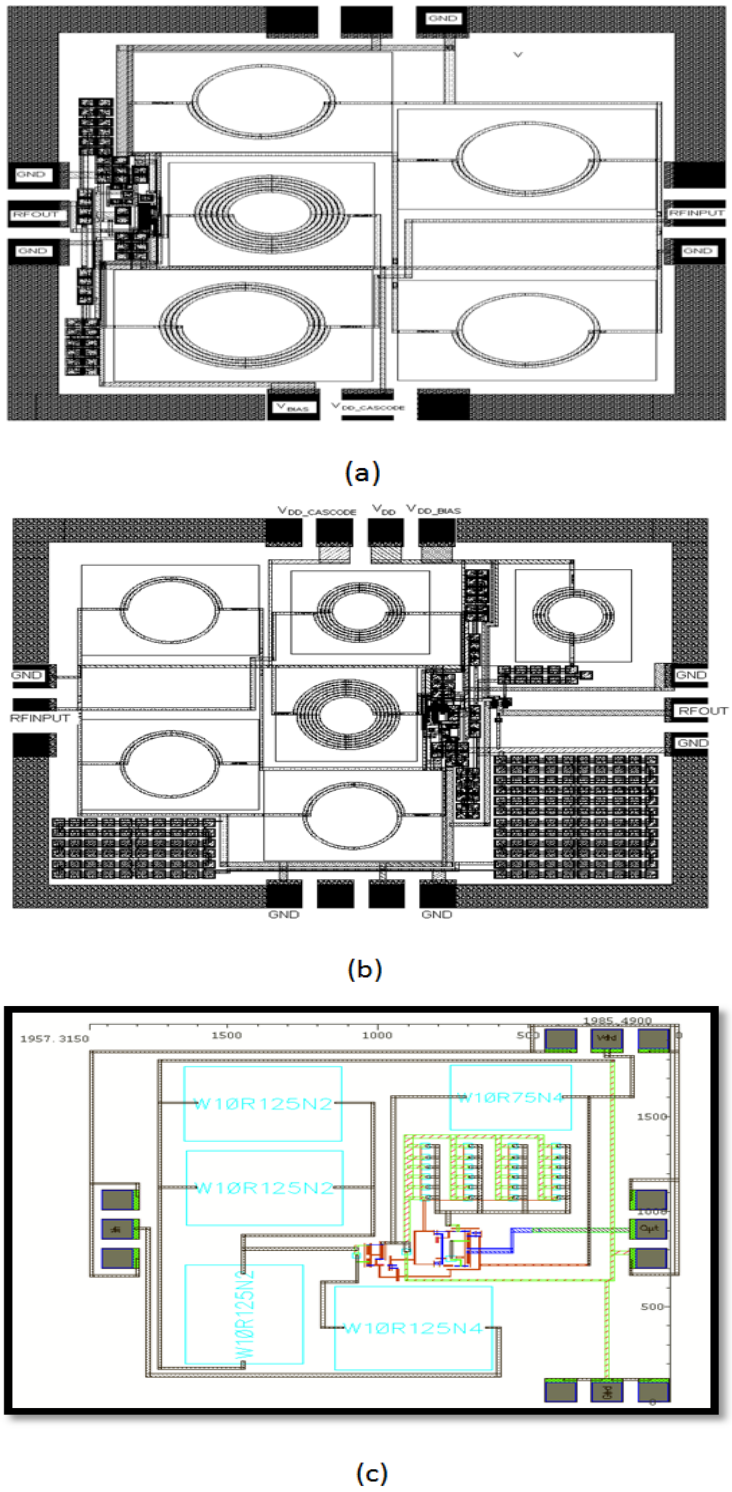

Figure 11: The layout of the LNAs; (a)PCSNIM, (b)PCSNIM with CD buffer and (c)PCSNIM with Class AB voltage follower

Table 3: Performance of LNAs with buffer from work by others. "na" means not available

Work by others	[9]	[10]	[11]	[12]	[13]
Buffer Type	Unity-gain AB	Single-ended CD	Single-ended CD	Single-ended CD	Single-ended CD
Result Type	Meas.	Meas.	Simu.	Meas.	Simu.
S_{11} (dB)	na	<−8	−36.3	<−9	<−10.3
S_{12} (dB)	na	<−40	−53.6	na	na
S_{21} (dB)	15.6	13	20.7	9.8	8.6-9.5
S_{22} (dB)	−32.4	<−14	−21.1	<−11	<−11.8
NF (dB)	2.2	na	3.0	2.3	2.7-3.2
NF_{min} (dB)	1.9	3.5	na	na	na
IIP_3 (dBm)	−3.2	−6.1	−14	−7	na
P_{1dB} (dBm)	−15.2	−15.4	−24	na	na
I_{buffer} (mA)	na	na	na	na	na
I_{total} (mA)	na	na	na	7	na
P_D (mW)	20	3.4	17.5	12.6	15
V_{DD} (V)	2.7	1.0	1.8	1.8	1.8
Freq. (GHz)	0.9	3.1-4.8	5.7	3-5	3-5
Tech. (nm)	500	130	180	180	180

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