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DEVELOPMENT OF THE OFFSET QUADRATURE PHASE SHIFT KEYING MODULATOR FOR ZIGBEE STANDARD ON FPGA

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Abstract—Zigbee is a standard that defines a set of communication protocols for low data rate short-range wireless networking. It operates primarily in the 2.4 GHz band, which makes the technology easily applicable and readily available worldwide. This paper provides a short overview of the Offset Quadrature Phase Shift Keying (OQPSK) modulator in the digital transmitter based on the Zigbee Standard. The use of Verilog code through Xilinx ISE is presented. The Verilog code is synthesized, simulated, and implemented on a Spartan3E XC3S500E Field Programmable Gate Array (FPGA). The design area of OQPSK modulator obtained is smaller than that of Very-high-speed integrated circuit Hardware Description Language (VHDL) based design. The OQPSK modulator functionality is illustrated through simulations and verified via measurements. The proposed design matches theoretical expectations. The implementation configuration requires approximately 26.1% of slices, 22.7% of flip-flops, and 15.2% of look-up tables (LUTs). With the clock frequency of 2 MHz, the synthesis run time took 93 s.

Keywords: Zigbee, OQPSK, Verilog, Xilinx, FPGA

1. INTRODUCTION

Nowadays, increasing attention has been focused on Zigbee, a low data rate, low power, and low cost wireless networking protocol based on the IEEE 802.15.4 standard for Wireless Personal Area Networks (WPANs). The standard specifies that a compliant system will operate in three license-free bands: 868 MHz (20 kbps) for North America, 915 MHz (40 kbps) for Europe, and 2.45 GHz (250 kbps maximum data rate) for worldwide use [1]. The transmission range is 10 to 100 meters based on the environment [2]. The major applications of Zigbee focus on sensor and automatic control, such as military application, industrial control, smart buildings, and environmental monitoring [3]. There are four packet frame types for the Zigbee Standard: data, acknowledgment, Media Access Control (MAC) command, and beacon. The beacon frame is used by a coordinator to transmit beacons. The function of beacons is to synchronize the clock of all the devices within the same network. The data frame is used to transmit data. Meanwhile, the acknowledgement frame is used to confirm successful frame reception [4]. The MAC commands are transmitted using a MAC command frame.

Previously, digital Offset Quadrature Phase Shift Keying (OQPSK) was designed either using Matlab, schematic or Very-high-speed integrated circuit Hardware Description Language (VHDL). For example, Jain et al. [5] developed and simulated the OQPSK modulator for CDMA system using Matlab. However, to the best of the authors knowledge, the modulator was not implemented in his work. Schematic on the other hand is not practical for a complex design because of longer design timeframe. In COM-101 [6], VHDL has been used to design the OQPSK demodulator through Xilinx ISE 4.1. The demodulator was then implemented on Spartan2 XC2S200 FPGA. However,

VHDL makes the instruction process more complex, requiring a larger design area. Hence, VHDL cannot be applied in the development of small size devices. In this paper, Verilog code is used as an alternative design methodology because it is simpler, more time-efficient, and optimal compared with VHDL. Although Li et al. [7] has designed the OQPSK modulator with the similar design method, the modulator has never been implemented.

Here, the code for OQPSK modulator is implemented on Spartan3E family FPGA, which is specifically designed to meet the high-volume and cost-sensitive needs of consumer electronic applications. Device enhancements, combined with advanced 90 nm process technology, deliver more functionality and bandwidth per dollar than was previously possible, setting new standards in the programmable logic industry [8].

This paper is organized as follows. In the second section, an overview of the Zigbee digital transmitter is given, followed by the characteristics of the OQPSK modulator in the third section. The fourth section explains the design methodology. In fifth section, the results and discussion of final simulation and measurement for the OQPSK modulator are presented. Finally, the paper is concluded in the sixth section.

2. OVERVIEW OF ZIGBEE TRANSMITTER

Sixteen channels are available for the 2.4 GHz band applications with ample channel spacing of 5 MHz. The Zigbee standard employs a Direct Sequence Spread Spectrum (DSSS) that uses a digital spreading function representing Pseudo-random Noise (PN) chip sequences [9].

This paper is focused on acknowledgment frame. Figure 1 shows the structure of the acknowledgment frame based on [4,10], which originates from within the MAC sub-layer. This frame is constructed from a MAC Header (MHR) and a MAC Footer (MFR). The MHR contains the MAC Frame Control field and the Direct Sequence Number (DSN), while the MFR is composed of a 16-bit Frame Check Sequence (FCS). Together, the MHR and the MFR form the MAC acknowledgment frame and passes to the Physical (PHY) as the PHY Service Data Unit (PSDU), which then becomes the PHY payload. The PHY payload is prefixed with the Synchronization Header (SHR) containing the Preamble Sequence and the Start of Frame Delimiter (SFD) fields as well as the PHY Header (PHR). The SHR, PHR, and PHY payloads form the PHY packet known as the PHY Protocol Data Unit (PPDU).

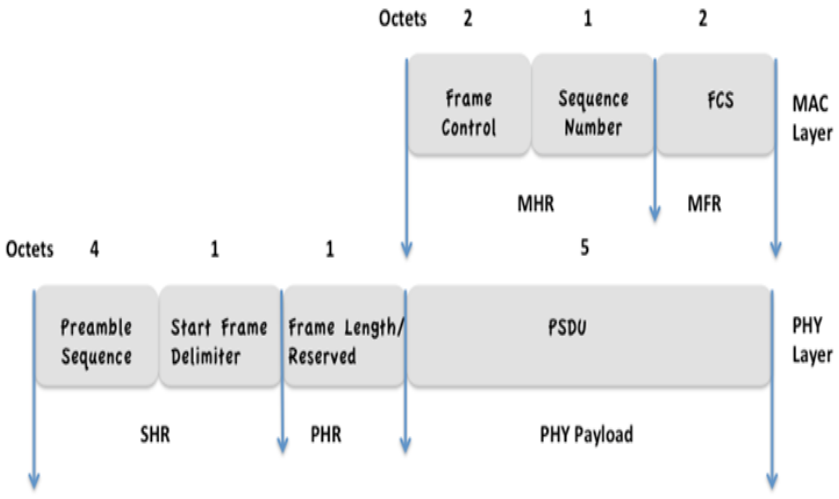

Figure 1: Schematic view of the acknowledgment frame and the PHY packet

In this paper, the Preamble Sequence contains 32 bits which are at logic '0'. For the SFD, the length is 8 bits with logic '1110 0101' as stated in the Zigbee Standard. The PHR also contains 8 bits in length with logic '1010 0000' [4]. The Frame Control is 16 bits in length with logic '0100 0100 0000 0000'. The Sequence Number logic is '1000 0000'. Finally, the FCS is 16 bits in length and contains the Cyclic Redundancy Check (CRC) algorithm that depends on the MHR. This gives a total of 88 bits for the acknowledgment frame.

Figure 2 shows the block diagram of the proposed Zigbee digital transmitter based on [10] and [11]. Binary data from the PPDU packet is inserted into the CRC block and then to the bit-to-symbol block. Then, every 4 bits are mapped into one data symbol. As shown in Table 1 based on [4], the symbol-to-chip block performs the DSSS where each symbol is mapped into a 32-chip PN sequence. The OQPSK modulation is adopted in the 2.4 GHz band.

The fundamental OQPSK method is to sum the in-phase signal with a quadrature phase signal delayed by half a cycle in order to avoid sudden phase shift change [11]. The modulated OQPSK signal then goes to the half-sine pulse shaping stage in order to reduce inter-symbol interference [12]. The resultant signal is transmitted by the Radio Frequency (RF) transmitter.

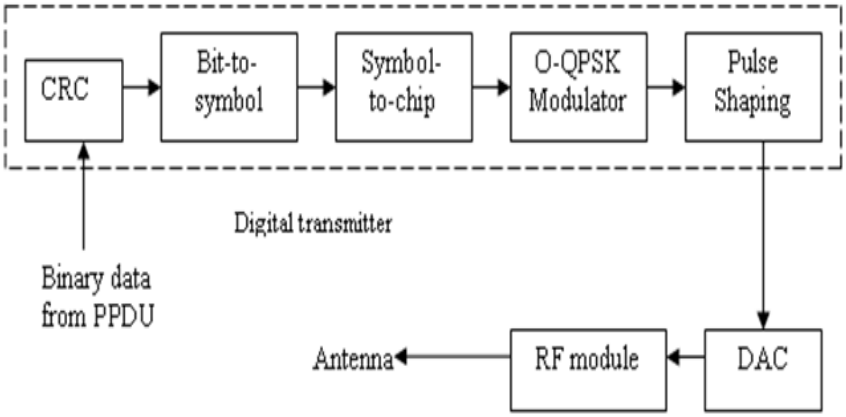

Figure 2: Detailed block diagram of the proposed Zigbee digital transmitter

3. OQPSK MODULATOR

The OQPSK modulator is an improved type of QPSK [7]. It is created from QPSK by delaying the Q channel by half a symbol from the I channel [13]. This delay reduces the phase shifts the signal goes through at any instant and results in an amplifier-friendly signal [14]. This OQPSK modulator design is created to meet the need for digital channel modulation in the 2.4 GHz band Zigbee transmitter.

At the OQPSK modulator stage, chip sequences representing each data symbol are modulated onto the carrier using OQPSK with half-sine pulse shaping. Even-indexed chips are modulated onto the in-phase (I) carrier and odd-indexed chips are modulated onto the quadrature-phase (Q) carrier. Figure 3 based on [4] shows that, to form the offset between I-phase and Q-phase chip modulation, the Q-phase chips shall be delayed by T_c with respect to the I-phase chips. T_c is the inverse of the chip rate. The chip rate is nominally 2 Mchip/s which is 32 times the symbol rate [15].

Table 1: Symbol to chip mapping using DSSS [4]

Data symbol (decimal)	Data symbol (binary) (b_0 b_1 b_2 b_3)	Chip values (c_0 c_1 ... c_{30} c_{31})
0	0 0 0 0	1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0
1	1 0 0 0	1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0
2	0 1 0 0	0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0
3	1 1 0 0	0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1
4	0 0 1 0	0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0 0 0 1 1
5	1 0 1 0	0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1 1 1 0 0
6	0 1 1 0	1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1 1 0 0 1
7	1 1 1 0	1 0 0 1 1 1 0 0 0 0 1 1 0 1 0 1 0 0 1 0 0 0 1 0 1 1 1 0 1 1 0 1
8	0 0 0 1	1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1
9	1 0 0 1	1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0 0 0 1 1 1 0 1 1 1
10	0 1 0 1	0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0 0 0 1 1 1
11	1 1 0 1	0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0
12	0 0 1 1	0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1 0 1 1 0
13	1 0 1 1	0 1 1 0 0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0 1 0 0 1
14	0 1 1 1	1 0 0 1 0 1 1 0 0 0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0 1 1 0 0
15	1 1 1 1	1 1 0 0 1 0 0 1 0 1 1 0 0 0 0 0 0 0 1 1 1 0 1 1 1 1 0 1 1 1 0 0 0

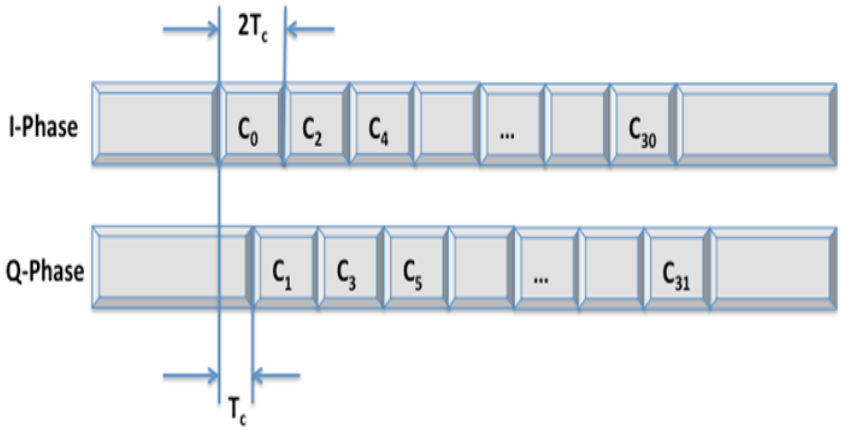

Figure 3: OQPSK chip offsets

4. DESIGN METHODOLOGY

The behaviour of OQPSK modulator, which is based on Table 1, was performed with Verilog through Xilinx ISE. The code was then synthesized in order to convert the code to the logic gates and check the design syntax to find any errors [16]. The simulation waveform was presented before the

implementation process purposely to ensure that the design's output waveform matches theoretical expectation. After the modulator was implemented onto the Spartan3E FPGA, it was measured using Logic Analyzer, as shown in Figure 4, once again to ensure that the design's output waveform matches the simulation waveform.

The proposed Verilog implementation for OQPSK modulator is best described as below.

1. The input data to this block are totally 704 chips per acknowledgment frame. These chips were obtained from equation (1) [17],

$$[88 \ \text{bits} \div 4 \ \text{symbols}] \times 32 \ \text{chips} = 704 \ \text{chips} \tag{1}$$

   The clock frequency is 2 MHz.
2. The input chips were divided into the odd and even chips, which were then stored in Q-phase and I-phase registers, respectively.
3. The 352 chips from I-phase registers were shifted serially to the output port followed by the 352 chips from Q-phase registers after a half clock cycle, T_c.

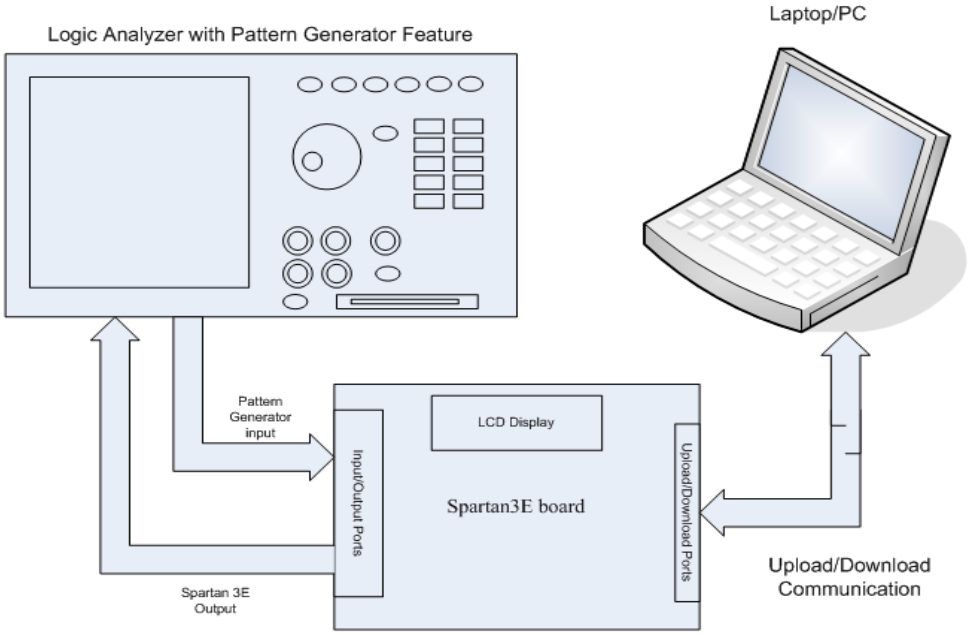

Figure 4: The measurement setup for OQPSK modulator

Figure 5 shows the schematic of OQPSK modulator. The *clk* is the clock frequency of 2 MHz. Meanwhile, the *data_in*, *load_mod*, *process_start*, *reset_mod*, and *shift_en* are the input ports. The *data_out(0)* and *data_out(1)* are the output ports for I-phase and Q-phase, respectively.

One part of the Verilog code for the OQPSK modulator is shown in Figure 6. The code was synthesized, simulated, and implemented onto FPGA to verify functionality.

5. RESULTS AND DISCUSSION

Simulation and measurement were carried out for the OQPSK modulator and the results were compared to verify its functionality. The logic values of 88 bits are based on the Zigbee Standard.

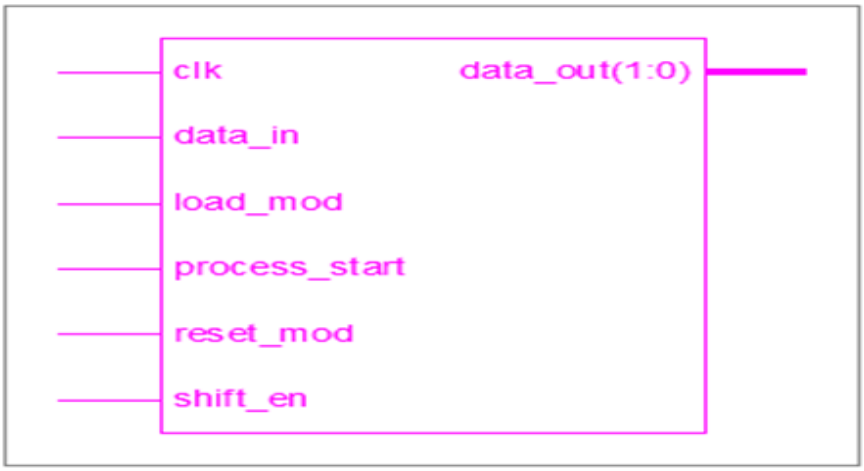

Figure 5: The structure of OQPSK modulator

```
module modulator(data_in, load_mod, reset_mod,
shift_en, process_start, clk, data_out);
input data_in, load_mod, reset_mod, shift_en,
process_start, clk;
output [1:0] data_out;

reg [704:1] count_in;
reg [705:0] count_even;
reg [705:0] count_odd;
```

Figure 6: The Verilog code for OQPSK modulator

5.1. Simulation Waveform

As shown in Figure 7, when only *shift_en* is at logic '1', the *data_out* is available within 352 500 ns, including the delay of T_c which occurred on odd chips. Logic values at both *data_out(0)* and *data_out(1)* are based on chip values contained in Table 1.

By referring to Figure 8, at 355 250 ns, the *data_out(1)* (Q-phase chips) is delayed by T_c=500 ns with respect to the *data_out(0)* (I-phase chips). The timing for each chip is $2T_c = 1\mu$s.

From the final simulation waveform, output data of the OQPSK modulator is shown to match theoretical expectation.

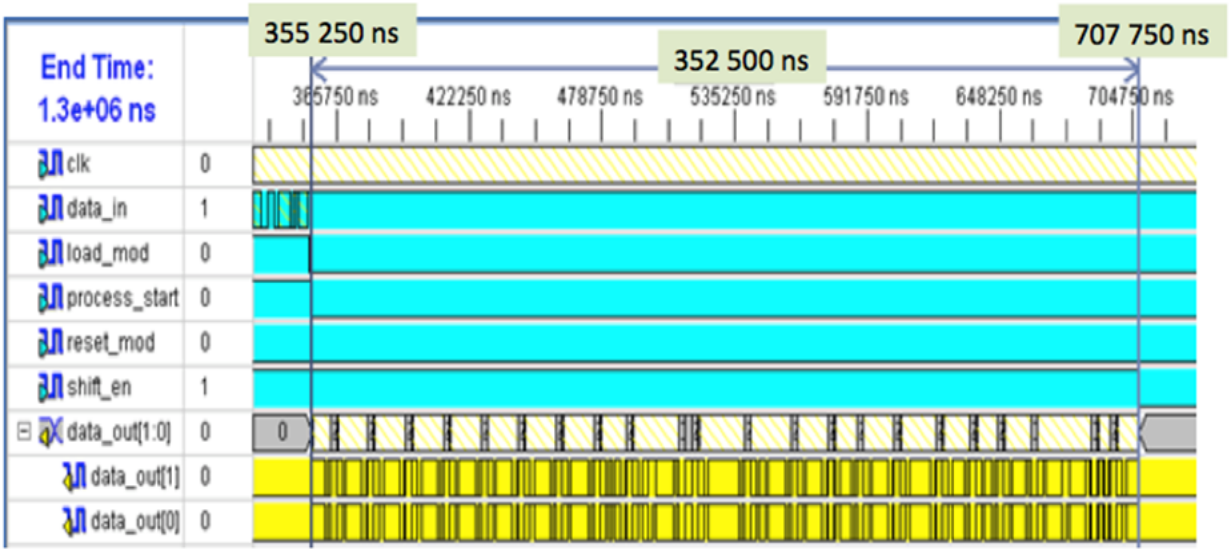

Figure 7: The simulation waveform of output data

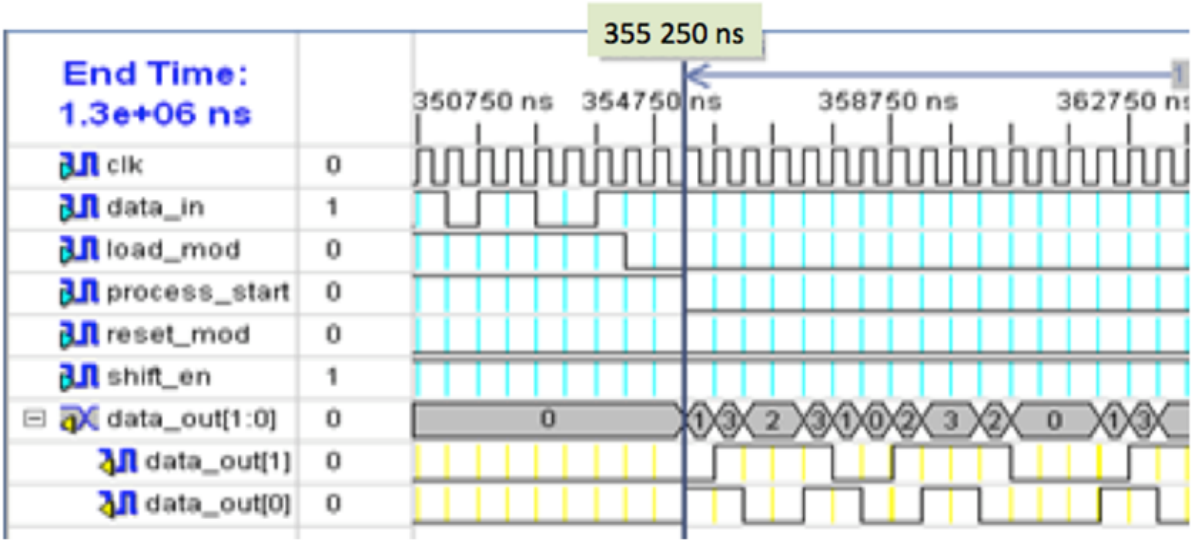

Figure 8: The simulation waveform of *data_out(0)* and *data_out(1)*

5.2. Measurement Result

Figure 9 shows that when only *shift_en* is at logic '1', the *data_out* is available within 352 497 ns from M1 to M2, including the delay of T_c which occurred on odd chips. Logic values at *Data1* are referred to *data_out(0)*, and *Data2* is referred to *data_out(1)*. Both *Data1* and *Data2* are similar to the output data in simulation waveform.

From Figure 10, it can be seen that *Data2* (Q-phase chips) is delayed by $T_c \approx 500$ ns from M3 to M4, with respect to *Data1* (I-phase chips). The waveform also shows that the minimum output delay after clock is 1.667 ns while the maximum output delay after clock is 18.333 ns. The timing for each chip is approximately 1μs.

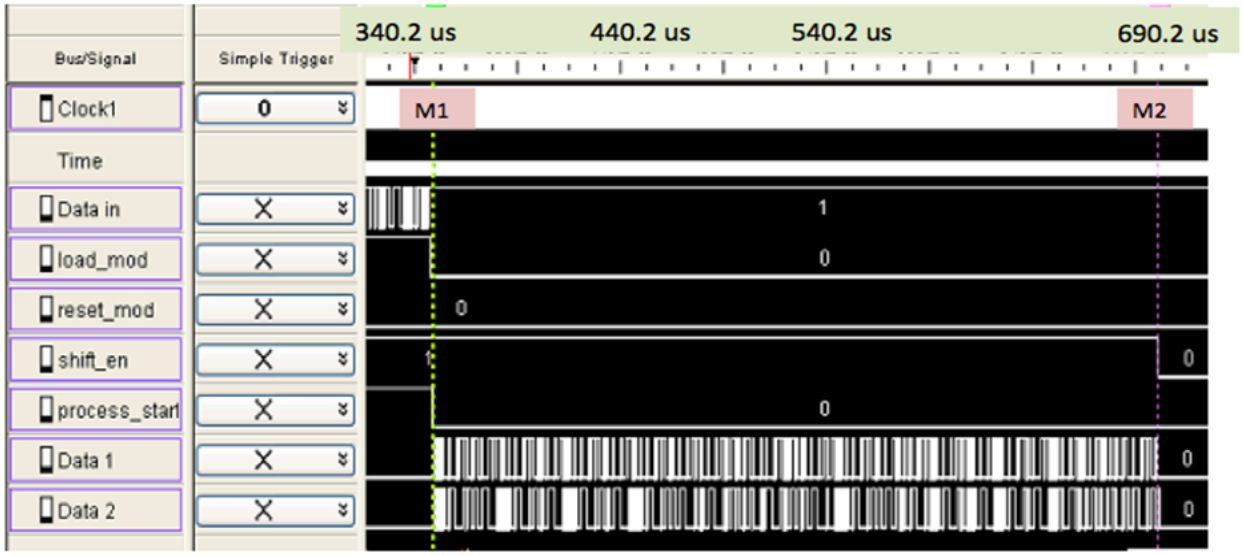

Figure 9: The measurement waveform of output data

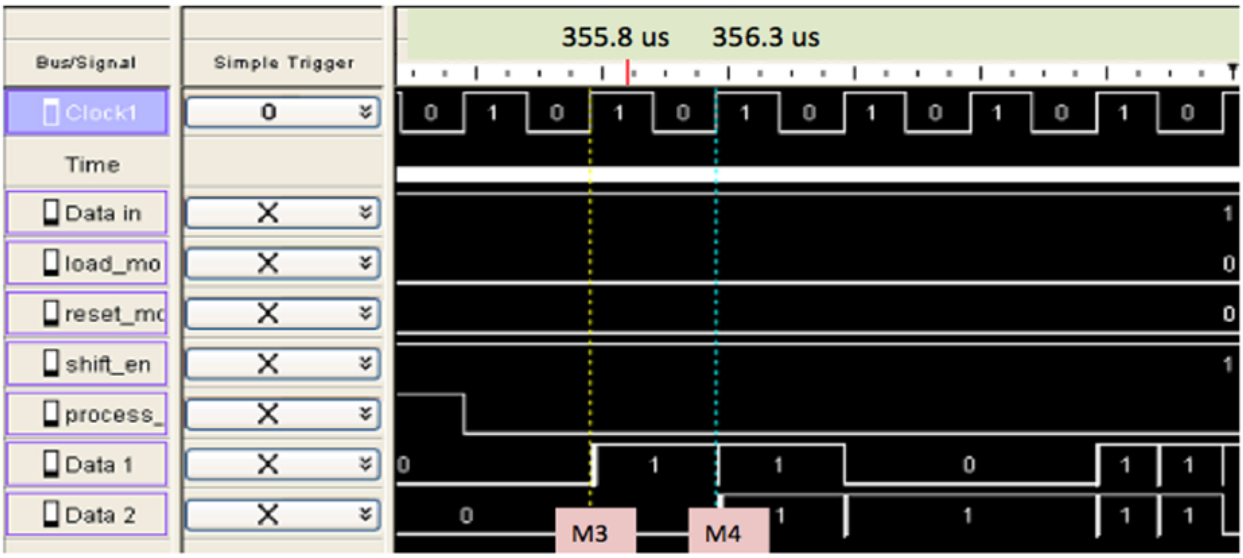

Figure 10: The measurement waveform of *Data1* and *Data2*

The measurement result shows that output data of the OQPSK modulator match the final simulation waveform. However, the measurement waveform shows that a small delay occurred at *Data1* and *Data2* after the rising edge of a clock. The delay is most probably caused by pin and net delays on Spartan3E FPGA. As the modulator was implemented with a speed grade of 5, the specifications obtained after implementation is summarized in Table 2. Specifications for the VHDL-based design methodology are included for comparison. The table shows that the configuration required about 1 216 slices out of 4 656 (26.1%), 2 115 flip flops out of 9 312 (22.7%), and 1 415 look-up tables (LUTs) out of 9 312 (15.2%). The average connection delay for this design was 1.630 ns. All signals were completely routed within 93 s with 194 MB CPU memory

usage. These results show that the total of slices, flip-flops, and LUTs for Verilog-based OQPSK modulator decreased by 73%, 40%, and 62% respectively as compared to implementation of VHDL-based OQPSK demodulator. Therefore, it is proven that the design area of OQPSK modulator with Verilog-based design method is smaller than to VHDL-based method.

Table 2: Comparison between the proposed design method and the VHDL-based design method

Specifications	Proposed Design Method		VHDL-based Method [6]*	
	Numbers involved	Percentage (%)	Numbers involved	Percentage (%)
Slices	1 216	26.1	2 350	99
Flip-flops	2 115	22.7	2 998	63
LUTs	1 415	15.2	3 645	77

(*Note: The VHDL-based design involved OQPSK demodulator.)

6. CONCLUSION

This paper describes the development of an OQPSK modulator as part of the digital transmitter for a 2.4 GHz band Zigbee Standard on FPGA. This modulator is used to sum the in-phase signal with a quadrature-phase signal delayed by half a cycle in order to avoid sudden phase shift change. Verilog code is used to characterize the OQPSK behavior, which is then simulated, synthesized, and successfully downloaded on Spartan3E FPGA. The measurement result shows that functionality of the OQPSK modulator matches theoretical expectation. Furthermore, the Verilog-based OQPSK modulator contributes to a smaller design area of FPGA device, compared to VHDL-based OQPSK demodulator. The design has been verified with the frequency of 2 MHz.

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